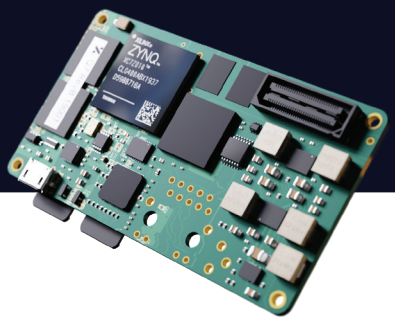


Q7 SPECIFICATIONS

FEATURE HIGHLIGHTS

INDUSTRY LEADING PERFORMANCE

The Q7 features an All Programmable System on Chip (AP SoC), including multi core CPUs supported by programmable logic resources and a wide array of hardware interfaces.

LOW MASS, VOLUME, POWER

The Q7 measures 78 mm x 43 mm x 9 mm, has a mass of 24 g (excluding connectors) and consumes 2 W for typical applications. Its small size, low mass and power consumption make the Q7 ideal for aerospace applications.

INTEGRATED HYBRID ENVIRONMENT

The application space in a Q7 is a tight integration of dual ARM Cortex A9 MPCore processors and programmable logic, featuring 106,400 flip flops and 53,200 lookup tables reserved for application-specific use.

FLEXIBLE INTERFACING

The Q7 provides Gigabit Ethernet networking through its RJ45 connector and USB 2.0 Host port. The Q7 also provides multiple digital I/O lines, including up to 24 LVDS pairs, and selectable RS-232/422/485 through its mezzanine connectors.

PRODUCT INTEGRATION MODULE (PIM)

Each Q7 is delivered with a detachable PIM to facilitate development. The PIM provides standard commercial interfaces (e.g. CAN, RS-232/422/485, 1-Wire, 12 GPIO, 4 analog inputs, JTAG), debug LEDs, and other lab development features.

SOFTWARE DEVELOPMENT

Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. Code previously developed for Linux desktop and server applications can be easily ported to the Q7. Q7 hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

LOGIC DEVELOPMENT

Logic development uses standard Xilinx development tools. Xiphos, Xilinx, and many third party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

FAULT HERITAGE

The Q7S, the Flight Model (FM) of the Q7, has been operating in orbit since June 2016. The Q7S is certified for manned space flight and is used on the International Space Station

Other flight heritage products in the current Xiphos Q-Card family include the Q8S and Q8JS

Xiphos has been flying previous generations of the Xiphos Q-Card family since 2002

FAULT TOLERANT

Fault tolerance features include:

Q7 can detect and correct faults within itself

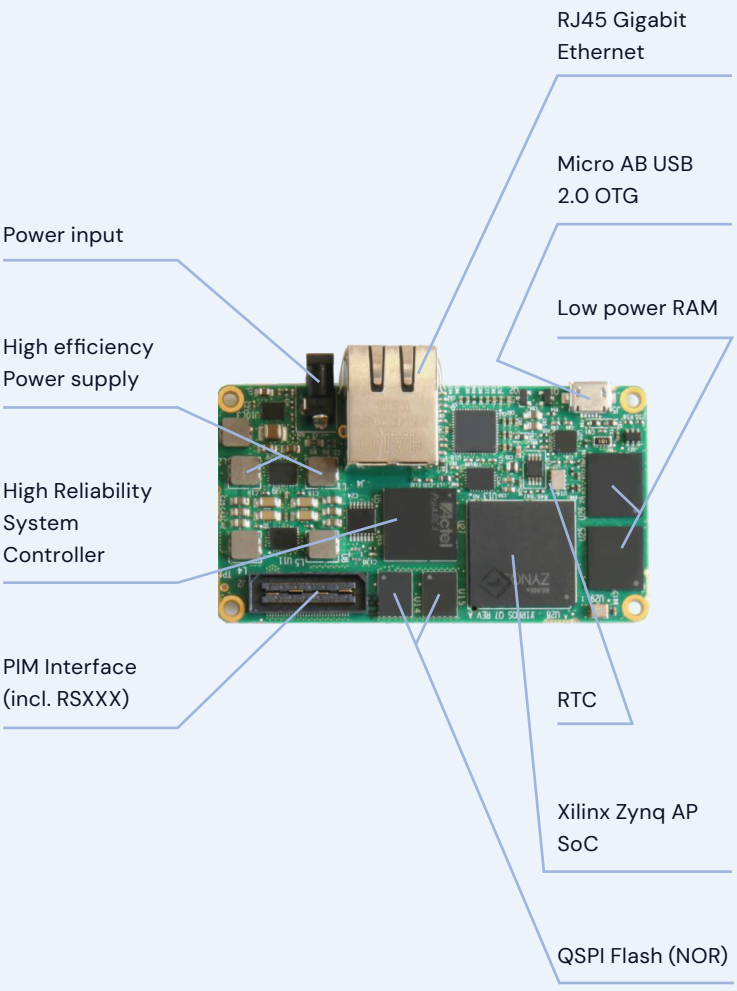
Combination of software and logic processing creates an excellent fail safe environment; logic can also be made triple mode redundant (TMR)

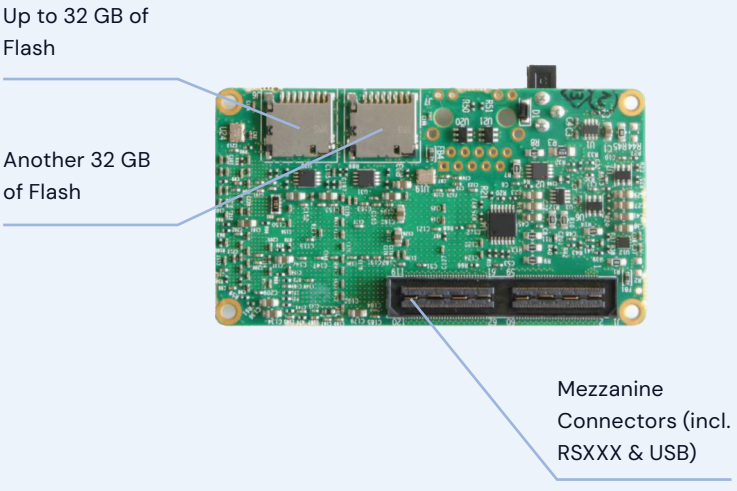
TMR logic in flight model version of Contro FPGA (Q7S)

EDAC on RAM

Redundant QSPI NOR Flash and MicroSD

FRONT & BACK





CHARACTERISTICS

MEMORY
- Independent 1x 512 MB (256MB with EDAC) and 1x 256 MB LPDDR2 RAM chips
- 2x 128 MB QSPI Flash (NOR)
- 2 MicroSD slots (max. 32 GB each) on independent buses / power control

ALL-PROGRAMMABLE SYSTEM-ON-CHIP
- Xilinx Zynq 7020
- Dual core ARM Cortex A9 MPCore processor at up to 766 MHz
- 106,400 flip flops (FF), 53,200 lookup tables (LUT), and 220 DSP slices

CONTROL FPGA
- Microchip ProASIC3

OPERATING SYSTEM
- Yocto Linux BSP (LTS distribution)

REAL TIME CLOCK (RTC)
- RTC with sleep & wake up on alarm/interrupt
- Dedicated power pin for external battery

POWER
- Scalable, typ. 2 W
- 6 V to 15 V (5 V to 28 V option)
- Power modes (including deep sleep)
- Overcurrent detection and protection

MASS
- 32 g with RJ45 connector
- 24 g without RJ45 connector

FORM FACTOR
- 78 mm x 43 mm x 19 mm (with RJ45 connector)
- 78 mm x 43 mm x 9 mm (without RJ45 connector)

ENVIRONMENTAL
- Operating Temperature -40 to +60C

INTERFACES
- Gigabit Ethernet (RJ45)
- USB 2.0 Host port (Micro AB)
- CAN Bus controller (in logic)
- Up to 58 single-ended GPIO, 23 MIO, 24 LVDS pairs/48 single-ended GPIO, USB 2.0, and factory-selectable RS-232/422/485 (Mezzanine connector)

Q7S FLIGHT MODEL INCLUDES
- Space-qualified software and logic
- Triple mode redundancy in Control FPGA
- EDAC-protected RAM
- Upset and multi-current monitoring
- FPGA bit stream scrubbing
- Software robustness / watchdog

xiphos.com
sales@xiphos.com

3981 St-Laurent Boulevard, Suite 500,
Montreal, Quebec, H2W 1Y5, Canada

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