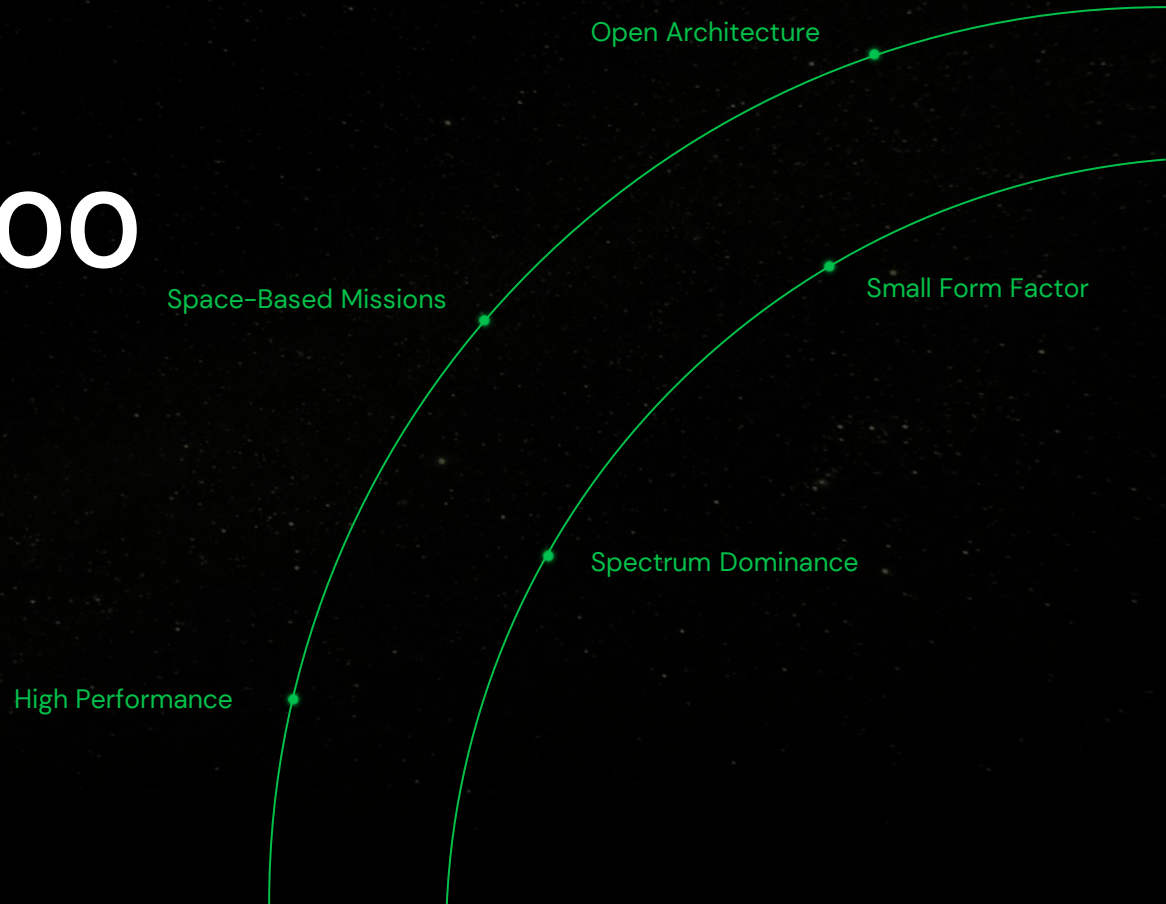
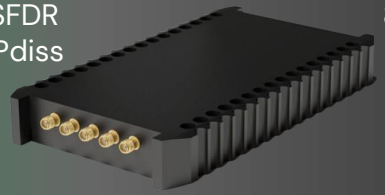
Sidekiq NV800



Low SWaP SDR Platform Products

Scalable SWaP vs Capability

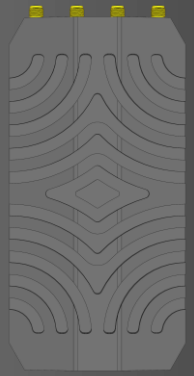
V40 Concept
1MHz – 9GHz
1R1T or 2R2T
50MHz - 1GHz+ BW
70dB SFDR
<40W Pdiss



NDR325
20MHz – 6GHz
Four Rx
500MHz BW
80dB SFDR
67W Pdiss

Z3u
45MHz – 6GHz
2ROT or 1R1T
50MHz BW
AMD Zynq US+ ZU3
GPSDO
<6W Pdiss

Z4 Concept
10MHz – 6GHz
Four Rx Four Tx
50MHz BW
70dB SFDR
<15W Pdiss



NV800
10MHz – 6GHz
Eight Rx
50MHz BW
70dB SFDR
<30W Pdiss

Z2
45MHz – 6GHz
1R1T
50MHz BW
AMD Zynq 7010
~2.5W Pdiss

SWaP

Capability

Sidekiq NV800 SDR – Funded by US DoD

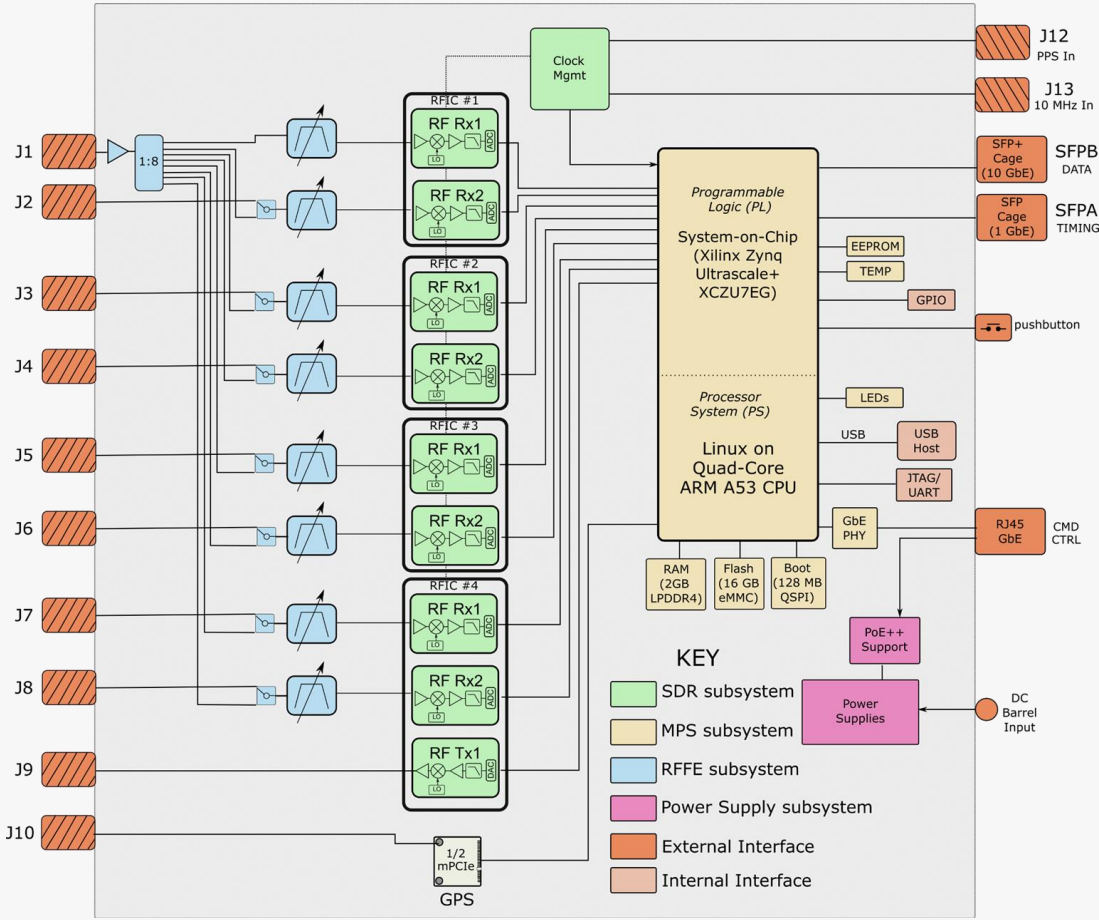
Standalone SDR Platform

- Eight RF Receivers in a Single SDR Platform
- 10MHz – 6GHz Tuning Range
  - Potential Extension to 18GHz on One Channel
- Phase Coherent or Independently Tuned Receivers
- 50MHz Bandwidth per Receive Channel, 16b ADCs
- 10GbE SFP+ Port for Streaming VITA 49
- 1GbE for Command & Control
- Integrated Support for WhiteRabbit (IEEE 1588-2019)
  - Enables <1ns Sync Between Remote Sensors
- Integrated 10MHz and PPS Inputs
- <30W Typical Power, Passively Cooled Housing
- Dimensions 9.92" x 7.24" x 2.0"
  - 25.2 x 18.4 x 5.1 cm
  - 144 inches^3, 2,365 cm^3

Detailed NV800 Block Diagram

External Interfaces

- 6-18GHz Extension: Currently Unpopulated
- J1: Can Feed All RFICs or Just RFIC #1 Rx1
- J2-J8: RFIC Rx Inputs or Unused
- J9: Single Tx Output
- J10: Connected to ½ MiniPCIe Connector
  - Populated with ½ Size GPS/GNSS Rx
- J12: PPS Input
- J13: 10MHz Input
- SFPB: 10GbE for IQ Data
- SFPA: WhiteRabbit or Additional 10GbE for IQ Data
- GPIO: 8 Externally Exposed GPIO Signals
- RJ45: 1GbE for Command & Control
  - Can Also Source POE++ for Power
- DC Barrel: Power Input if POE++ Not Used



NV800 RF Front End

Two Input Modes

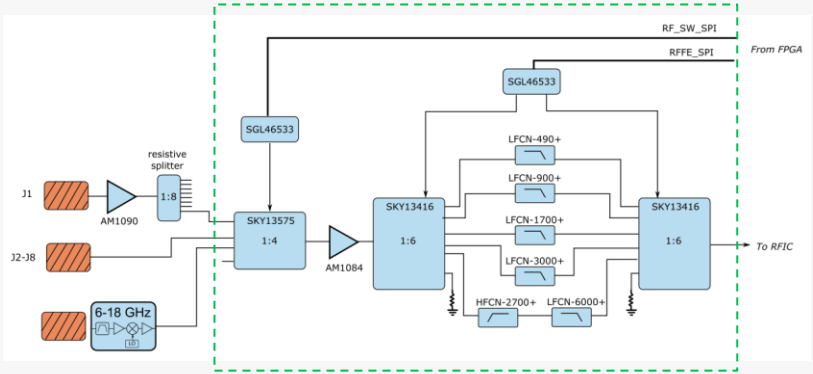
- Single Antenna Mode
  - J1 Connects to Antenna
  - Resistive Splitter Sends Signal to Every RFIC Rx Input
  - RFICs Can Still be Tuned Independently or Coherently
- Multiple Antenna Mode
  - J1 to J8 Each Connect or Antennas
  - Each Antenna Sends Signal to One RFIC Rx Input
  - RFICs Can Still be Tuned Independently or Coherently

On Card Signal-Conditioning

- Amplification, AM1090 and AM1084
- Filtering, Pre-Selection Bank
- Future Option to Have 18GHz Input to One RFIC
  - Block Conversion, Amplification, Filtering

Target RF Specs

- Gain = 20dB, NF = 7dB, IIP3 = +5dBm



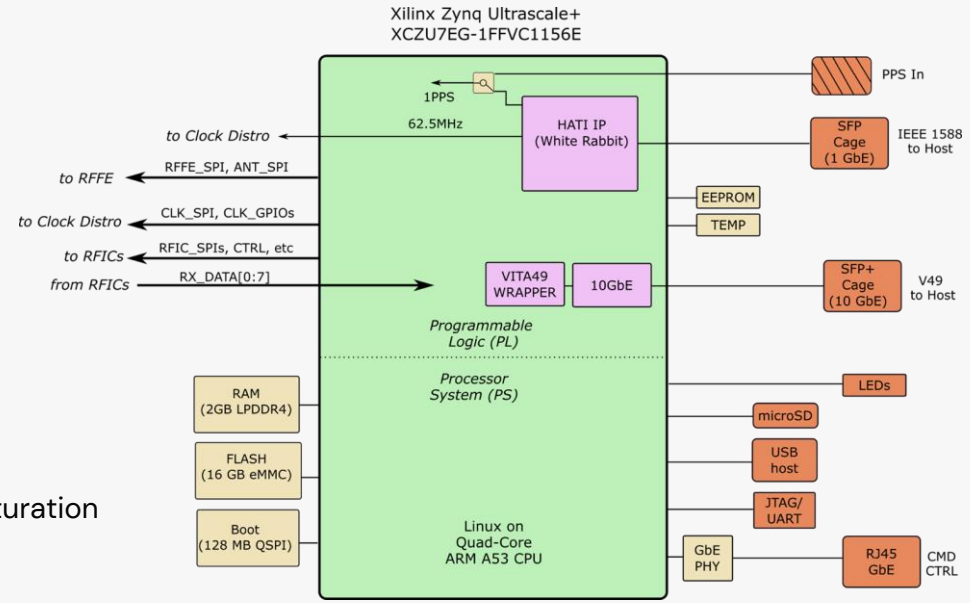
Future Extension

Eight Copies, One for Each RFIC Input

NV800 FPGA Subsystem

Two FPGA Modes

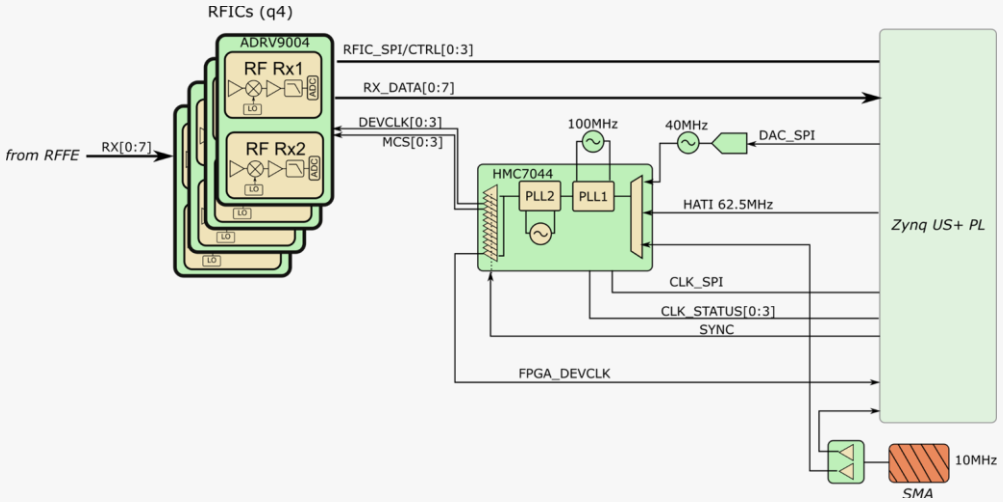
- Epiq Application – VITA 49 IQ Streaming
  - Epiq Provides FPGA Binary to Configure System
  - User Can Set Each RFIC IQ Streams (8x)
    - Sample Rate
    - Packet Size (Up to 9kb Jumbo Frames)
    - VITA 49 Stream IDs (V49)
    - Source and Destination
      - MAC (with Broadcast Ability)
      - IP Addresses (IP)
      - Port (UDP)
  - Full Rate VITA 49 Data Streams on 10GbE up to Link Saturation
- User Application
  - User Must Provide FPGA Binary
  - Epiq will Provide FPGA Source as Reference
  - User Registers in PL
  - User App Runs in PS to Configure PL
  - Reduced or Full Rate IQ Data Sta Streams on 10GbE
    - Still Uses VITA 49 Packets



NV800 RFIC & Clocking Detail

Three Clocking Modes

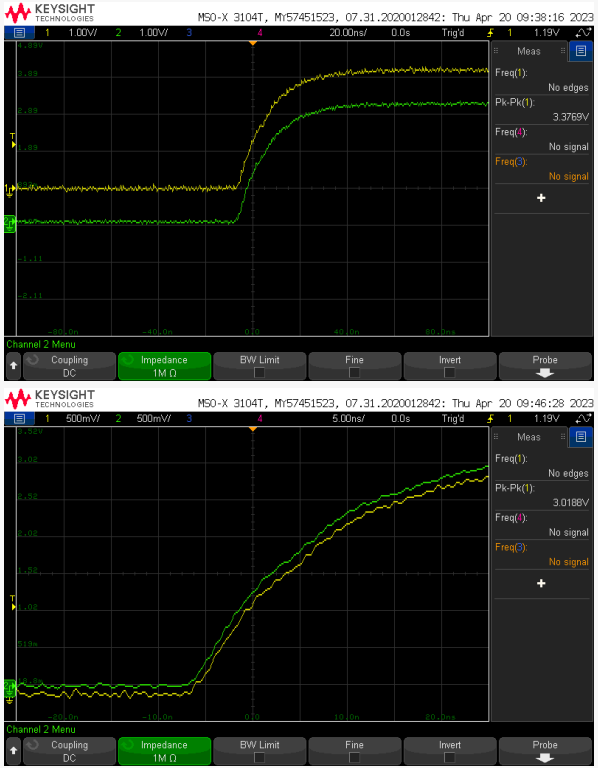
- External 10MHz
  - User Provides 10MHz Clock on J13
- WhiteRabbit
  - WhiteRabbit (IEEE 1588-2019) Signals of SFPA
  - FPGA will Product HATI 62.5MHz Clock
- On Board 40MHz Oscillator
- Warpable Thru SPI Controlled DAC



All Three Clock Sources Input to HMC7044

- 100MHz Reference Clock Always Delivered to RFICs
  - Potential Future Upgrade to 200MHz
- RFIC can Generate Internal Clocks
- Arbitrary IQ Rates are Supported from Single Reference Clock

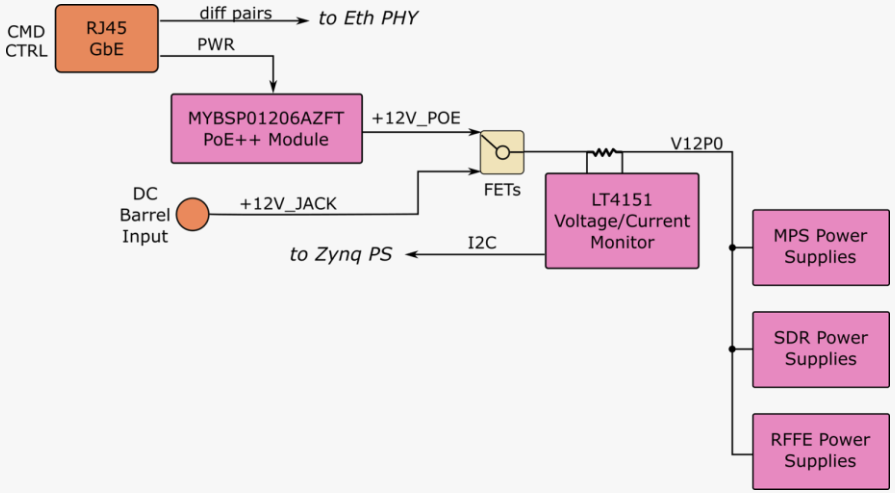
Early WhiteRabbit Results: <1ns PPS Alignment



NV800 Power Distribution

Two Power Modes

- POE++ is Primary Mode
- Power Delivered on 1GbE
- Max Power Handling is 40W
- DC Barrel Input is Secondary Mode
- 12V Input



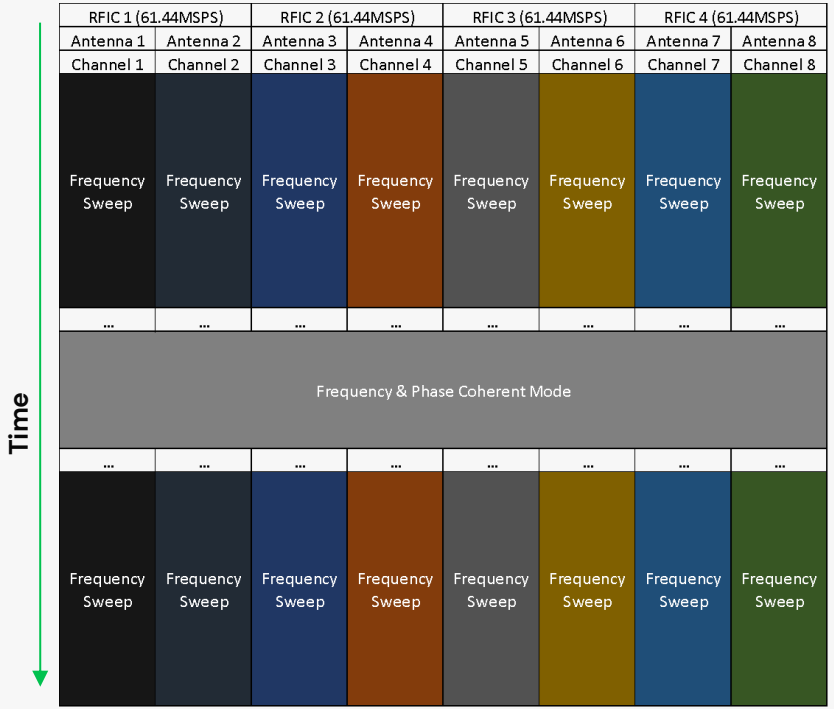
Total Power Estimated at <28W in VITA 49 Mode

Device	Power	Device	Power
FPGA	6.5W	DDR	1.2W
RFICs	7.6W	Power Supply	4.0W
HMC7044	1.5W	Ethernet PHY	0.5W
RF Front End	4.0W	Misc	0.7W
SFP+	2.0W	Total	28.0W

NV800 Software Control & Operating Modes

RFIC Software Control

- ERFS: **E**mbedded **RF** **S**erver
  - Abstracts RFIC Control
  - Receivers are Numbers 1 Through 8
  - Receivers can be Tasked with Stare or Sweep
  - Gain Control Unique to Each Sweep Step
- Multiple Operating Modes Available
  - Sweep & Stare Modes on Each Rx
  - Independent Sweep on Each Rx
  - Coherent Sweep on Each Rx
  - Independent Fixed Frequency on Each Rx
  - Coherent Fixed Frequency on Each Rx
  - Simultaneous Sweep & Stare Across the Rx Channels
  - Rx 1-4 as Coherent Block and Rx 5-8 as Coherent Block



NV800 Frequency Hopping

LO Tune Time – Currently 70µs

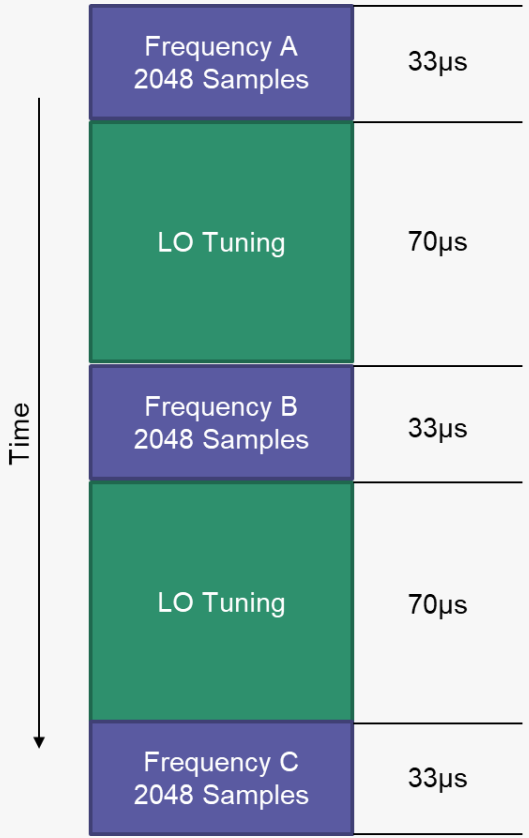
- Total Time Required to Change LO Frequency
- IQ Data is Blanked During this Time

Dwell Time – Configuration Dependent

- Total Time a Receiver will Stay on a Frequency
- Must Be a Multiple of the VITA 49 Sample Count
- Example, if VITA 49 Sample Count = 2048
  - @ 61.44MSPS IQ Rate, Minimum Dwell = 33µs

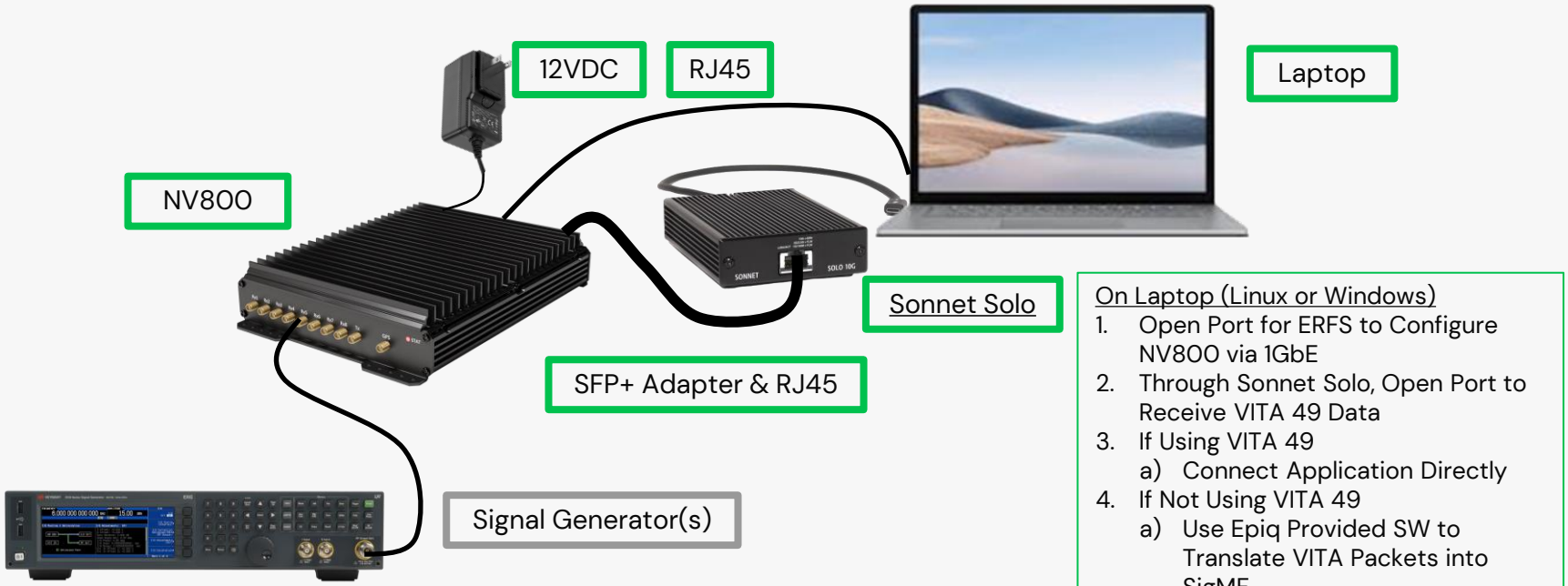
Fast Hopping Example

- IQ Rate = 61.44MSPS, BW = 50MHz
- VITA 49 Sample Count = 2048, Minimum Dwell is 33µs
- Sweep from 30MHz→6GHz
  - Total of 120 Steps at 50MHz Step Size
- Full 6GHz Sweep Takes 12.4ms
  - **Approximately ~481GHz/sec Coverage**



NV800 Demo & Evaluation

Epiq Provided | Customer Provided



On Laptop (Linux or Windows)

1. Open Port for ERFS to Configure NV800 via 1GbE
2. Through Sonnet Solo, Open Port to Receive VITA 49 Data
3. If Using VITA 49
   a) Connect Application Directly
4. If Not Using VITA 49
   a) Use Epiq Provided SW to Translate VITA Packets into SigMF
   b) Plot SigMF Data Using matplotlib or Other FFT Tool

Thank You

Wyatt Taylor
wyatt.taylor@epiqsolutions.com