SDR ARCHITECTURE COMPARISON

We've written elsewhere[1] about how UxS (Unmanned Systems) power budgeting is like squeezing a balloon between the required frequency range, RF performance, number of channels and processing, which all have a big impact on power consumption, heat dissipation, and ultimately achievable range. Our business primarily focuses on smaller platforms where the constraints are at their most extreme. We are technology agnostic, but having such a clear focus guides the choices and trade-offs we make in our designs. This short note describes some of these.

Figure 1 shows some of the key functional blocks and attributes of typical SDRs used for military purposes. The primary signal chain architecture used to be the superhet, using lots of exquisite gold bricks and yielding the absolute best performance. Recent years have brought alternative technology approaches and applications such as small UxS platforms, where the best answer can be 'good enough' performance in order to maximize other desirable traits.

The table of ***Figure 2*** compares the superhet approach with the more recent direct sampling architecture commonly used by RF System on Chip[2] products, and

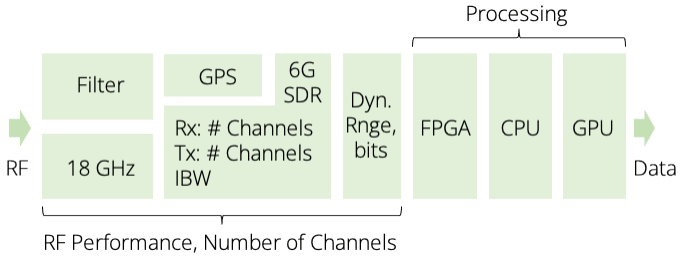

Figure 1: Common SDR functional blocks and attributes

the homodyne or zero IF method often employed by RF Integrated Circuit[3] block diagrams. We frequently end up favoring the zero IF architecture for UxS applications, as we'll explain.

FPGA-based direct sampling systems have advantages in extremely wide instantaneous bandwidths (IBW), currently 4 GHz and rising, and extremely low latency, making them very suitable for DRFM (Digital Radio Frequency Memory) applications. However, for many UxS applications the lower RF performance and higher size, weight and power requirements are too high a price to pay. For example, a high-end direct sampling chip can dissipate more than 60W on its own. The extremely wide IBWs are an advantage in some applications but a liability

Attribute	Traditional Superhetodyne	Direct Sampling	Homodyne/ Zero IF
RF Performance	Best RF performance, spurious-free dynamic range (SFDR)	Sub-par RF performance but technology evolving	Optimized design trade-offs for performance vs. SWaP
Size	Larger, bigger components	Medium, most suited to modular open platforms	Smallest
Power	Take a lot of power	Power can vary widely with design implementation; requires a lot of cooling	Lowest power
Processing	Usually optimized for one application, Inflex-ible	Low latency; single size FPGA, inflexible; can be difficult to balance generated digital data with available processing	Flexible choices of FPGA size, added CPUs, GPUs sized as needed
Manufacturability	Hard to manufacture	Moderate	Optimized for ease of manufacture, leverages commercial manufacturing scale, surety of supply, fast ramp-up
Cost	Expensive	Less expensive	Optimized

Figure 2: Comparing RF architectures for UxS applications

in others as the whole architecture needs to be designed to deal with such high raw data throughput, otherwise the system is throwing data away and wasting power needlessly. We find direct sampling approaches offer more options and more flexibility, allowing a designer to tailor parameters to suit the power and space constraints of small systems. Even with the addition of circuitry such as switches, amplifiers, filtering, GPS and other functions, zero IF-based SDRs can enable tiny, frugal solutions with very good RF performance. IBWs up to 450 MHz are available, but for many applications 50-200 MHz is more than enough particularly when coupled with several channels that can be switched between phase coherent and independent operation for scanning different parts of the spectrum simultaneously.

With the pressure on UxS platform designers to deliver, another factor to consider is manufacturability. This favors the more recent IC-based technologies over the traditional superhet, and is something we put a lot of effort into to allow fast ramp-up and surety of supply.

Recently small CPU/GPU (Graphical Processing Unit) solutions have become available[4] that can be integrated with the RF front end to take more of the processing load. While CPU/GPUs are unlikely to excel in low latency DRFM applications, they are extremely good at the kinds of large matrix math multiplications needed for AI/ML (Artificial Intelligence/ Machine Learning). This can greatly simplify things for a system designer, as instead of off-boarding large streams of raw time-coded data, an SDR has the potential to deliver a thin pipe of pre-processed answers, such as bearing and range in a direction finding application.

The technology options we use continue to evolve, and the choices we make to deliver our SDRs are often complex. **Contact us** for more information on which approaches might best suit your needs or visit **our website**.

REFERENCES

1 Epiq UxS Topic Series “Squeezing the Balloon”.
2 For example: https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html
3 For example: https://www.analog.com/en/products/adrv9004.html#product-overview
4 For example: https://www.nvidia.com/en-us/autonomous-machines/embedded-systems/jetson-orin/

ABOUT EPIQ

Epiq Solutions develops cutting edge tools for engineering teams and government-focused organizations requiring situational awareness and detailed insight into their RF environments in order to identify and act against wireless threats.

www.epiqsolutions.com
sales@epiqSolutions.com
+1 847 598 0218

3740 Industrial Ave,
Rolling Meadows, IL 60008, USA