Sidekiq™ NV100

RF Transceiver • Low SWaP

HARDWARE USER MANUAL

V1.4 - MAY 25, 2022

CHANGELOG

Revision	Date	Description	Author
0.1	2020-10-07	Pre-release draft, initial version	Barry L
1.0	2021-10-13	First release	Barry L
1.1	2021-11-11	NUC PDK and JTAG fixture updates	Barry L
1.2	2022-01-11	Added power consumption numbers	Barry L
1.3	2022-02-11	Updated jtag fixture, rf port mapping, MTBF, and SoV tables, and format cleanup	Barry L
1.4	2022-05-25	Updated status LED table, added AppArmor note and GPSDO performance section	Barry L

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INTRODUCTION

This document provides an overview of Epiq Solutions' Sidekiq NV100 SDR, an M.2 card with integrated RF transceiver, FPGA, RF pre-selection filtering, GPSDO and PCIe interface to a host. This card is similar to the Sidekiq Stretch card developed by Epiq Solutions, but leverages the ADI ADRV9004 RFIC with higher performance 16-bit ADCs and DACs, improved linearity, lower RF frequency tuning, and is capable of supporting two main modes of operation: dual-independently tunable Rx, or Tx+Rx on the same frequency.

The following topics will be discussed:

- Overview of the Sidekiq NV100 hardware interfaces
- Sidekiq NV100 usage/integration options
- Sidekiq NV100 JTAG fixture usage
- Sidekiq NV100 NUC PDK

All documentation and support for Sidekiq NV100 is provided through Epiq Solutions' support website which can be found at: https://support.epiqsolutions.com

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq NV100 is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. Each user of Sidekiq NV100 and associated software is solely responsible for ensuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

Each Sidekiq NV100 unit is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq NV100 unit can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq NV100 from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

OVERVIEW

This guide provides an overview of the Sidekiq NV100 software defined radio hardware platform, associated capabilities, and basic usage. This includes the following:

- System level block diagram of the platform
- Overview of the externally accessible hardware ports
- Powering the system up and down

All documentation and support for Sidekiq NV100 is provided through Epiq Solutions' support website:

https://support.epiqsolutions.com

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

REFERENCES

1. **Sidekiq NV100 Product Page**

   https://epiqsolutions.com/rf-transceiver/sidekiq-nv100/

2. **Epiq Solutions Support Page**

   https://support.epiqsolutions.com

3. **ADI ADRV9004 Transceiver Product Page**

   http://www.analog.com/en/products/adrv9004.html

4. **u-blox ZOE-M8 GNSS SiP module**

   https://www.u-blox.com/en/product/zoe-m8-series

5. **Berquist Thermal Gap Pad Material**

   http://www.bergquistcompany.com/thermal_materials/gap-pad.htm

6. **PCI-SIG PCIe M.2 Specifications**

   https://pcisig.com/specifications/pciexpress/

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
BIOS	Basic Input/Output System
COTS	Commercial Off The Shelf
D/A	Digital to Analog converter
dB	Decibel
dBm	Decibels referenced to one milliwatt (mW)
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
GALILEO/BEIDOU	European Union's Galileo and China's BeiDou Navigation Satellite Systems
GHz	gigahertz
GLONASS	GLObal NAvigation Satellite System
GPIO	General Purpose Input / Output (I/O)
GPS	Global Positioning System
GPSDO	Global Positioning System Disciplined Oscillator
HDMI	High-Definition Multimedia Interface
IF	Intermediate Frequency
I/Q	In-Phase / Quadrature Phase
JTAG	Joint Test Action Group
kHz	kilohertz
LED	Light Emitting Diode
MHz	megahertz
MIMO	Multiple Input Multiple Output
ms	millisecond
NUC	Next Unit of Computing
NVMe	Non-Volatile Memory
PDK	Platform Development Kit
PID	Proportional–Integral–Derivative
PPS	Pulse Per Second

PPM	Parts Per Million
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RFFE	RF Front-End
Rx	Receive
SBAS	Satellite-based Augmentation System
SDK	Software Development Kit
SDR	Software Defined Radio
SSD	Solid-state Drive
TB3	Thunderbolt 3
TCVCXO	Temperature Compensated Voltage Controlled Crystal Oscillator
TDD	Time-division duplex
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
U.FL	Miniature RF coax connector, manufactured for use as the antenna interface on M.2 cards
USB	Universal Serial Bus
W.FL	Micro-Miniature RF coaxial connector manufactured by Hirose

Table 1: *Terms and Definitions*

SYSTEM OVERVIEW

Sidekiq NV100 is a miniature software defined radio card in a M.2 2280 card form factor, providing a flexible wideband RF transceiver that can be used by a host system. The M.2 2280 form factor is widely used for PCIe-based NVMe® solid state drives (SSDs) in commercial laptops, embedded systems and servers. The features of the Sidekiq NV100 include the following:

- Compliant with M.2 2280 card form factor (22mm x 80mm x 4.5mm), Module Key B+M
- RF transceiver covering 30 MHz to 6 GHz (RF access to 10 MHz), with independent Tx and Rx frequencies (Analog Devices ADRV9004 RFIC)
- Supports RF channel bandwidths up to 40 MHz
- Supports multiple RF modes:
  - *****Dual channel phase coherent Rx
  - Dual channel independently tunable Rx
  - Single channel Tx and single channel Rx
    - 1Tx + 1Rx (FDD, on different antenna ports)
    - 1Tx + 1Rx (TDD, on the same antenna port)
    - 1Tx + 1Rx (TDD, on different antenna ports)

**Dual channel phase coherent receive is currently in development and will be supported in a future software/firmware release. Contact Epiq Solutions support for further information.*

Receive only:

- Single channel receive
  - up to 40 MHz IBW
- *****Two phase coherent channel receive
  - up to 40 MHz IBW
- Two independently tunable channel receive
  - up to 40 MHz IBW each

Transmit only:

- Single channel transmit
- Dual channel transmit

Receive and transmit:

- Single channel TDD (TRX)

    - RxA1 / TxA1
- Dual channel, independently tunable TDD
    - RxA1 / TxA1 and RxB1 / TxB1
- Single channel FDD
- RxB1 / TxA1, indep tunable
- A/D and D/A quadrature sample rates from 24 Ksamples/sec up to 61.44 Msamples/sec, with 16-bit precision
- User programmable FPGA for signal processing applications (Xilinx Artix XC7A50T-2CPG236I)
- SPI flash for storage and automatic FPGA bitstream loading at boot-up
- Sub-octave Rx pre-select filtering for interference protection from 30 MHz to 6 GHz on each RF receiver
- Integrated GPS receiver with PPS for high accuracy
- On-board 40 MHz TCVCXO with +/- 0.1 PPM accuracy; support for optional external 10 MHz or 40 MHz reference clock input, software controlled
- PCIe Gen 2.0 (5 Gbps) x2 interface to the host platform
- Support for external 1PPS input signal for sample time alignment across multiple Sidekiq units
- Weight: 9 grams
- Power: 4 - 6 W (application dependent)

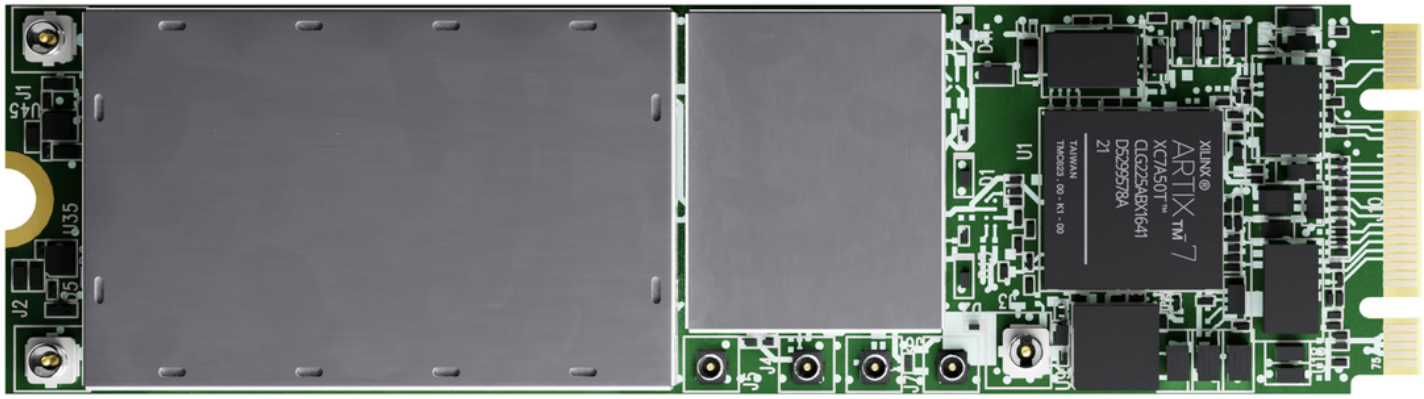

Figure 1: *Sidekiq NV100 front side*

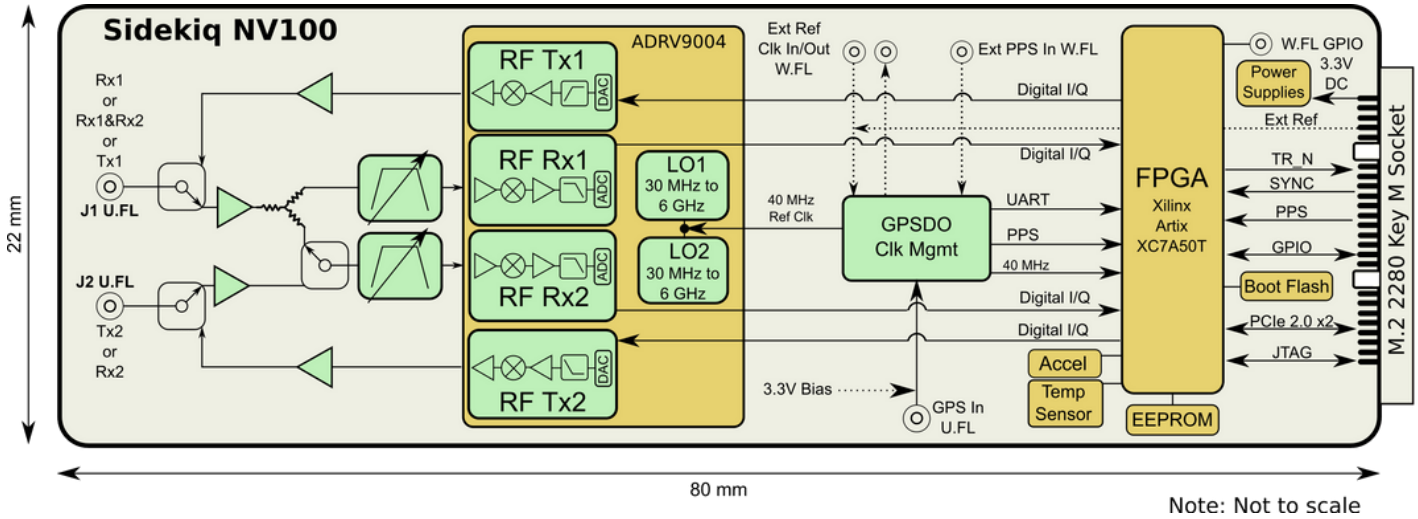

Figure 2: *Sidekiq NV100 block diagram*

HARDWARE SPECIFICATION

RF RECEIVER SPECIFICATION

RF Input	U.FL miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	30 MHz to 6 GHz (RF access to 10 MHz)
Tuning Step Size	~4.5 Hz
Tuning Time	Refer to Sidekiq Software Development Manual, Release 4.17.x or later - Methods of LO frequency tuning
Typical Noise Figure	< 5 dB
Typical IIP3	(J1) Rx1: 0 dBm (J2) Rx2: +9 dBm
Gain Control Range	0 to 34 dB, 0.5 dB steps
Gain control Modes	Manual or AGC
A/D Converter Sample Rate	24 Ksamples/sec to 61.44 Msamples/sec
A/D Converter Sample Width	16 bits
Typical I/Q balance	> 65 dB
Max. RF input signal (without damage)	+20 dBm
RF full scale input (at max gain)	-18 dBm on (J1) and -25 dBm on (J2), frequency dependent
RF Pre-Selection Filtering	Sub-octave pre-select filtering for interference protection from 30 MHz to 6 GHz; automatically selected when tuning the RF receiver.

Table 2: *RF Receiver Spec*

RF TRANSMITTER SPECIFICATION

RF Output	U.FL miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	30 MHz to 6 GHz (RF access to 10 MHz)
Tuning Step Size	~4.5 Hz
Tuning Time	Refer to Sidekiq Software Development Manual, Release 4.17.x or later - Methods of LO frequency tuning
Gain Control Range	0 to 48 dB, 0.25 dB steps
Max. RF Transmit Output Power	+5 dBm
Typical OIP3	30 dBm
D/A Converter Sample Rate	24 Ksamples/sec to 61.44 Msamples/sec
D/A Converter Sample Width	16 bits
Typical I/Q balance	> 60 dB

Table 3: *RF Transmitter Spec*

CLOCK/SYNCHRONIZATION SPECIFICATION

RF Input Port	U.FL miniature coaxial connector (50 ohms)
On Board Reference Clock	40 MHz, +/- 0.1 PPM accuracy, (shared with Rx & Tx) P/N: SiTime SIT5356
External Reference Clock Input Frequency	10 MHz or 40 MHz
External Reference Clock Input Power Range	0.8 – 1.3 Vpp, 0 dBm max from 50 ohm source for 40 MHz 0.8 – 3.0 Vpp, +7 dBm max from 50 ohm source for 10 MHz
Reference Clock Output Frequency	40 MHz
Reference Clock Output Power	~1.3 Vpp into high-Z load or ~635 mVpp into 50 ohm load
PPS Input Level	3.3V max.

Table 4: *Clock Spec*

HARDWARE SPECIFICATION

M.2 slot type	M.2 2280 B+M card form factor (22mm x 80mm x 4.5mm), Module Key B+M
FPGA	Xilinx Artix 7 XC7A50T-2CPG236I with x2 PCIe interface to host
FPGA Reprogramming	Over PCIe
FLASH	Micron 128Mb MT25QU128ABA1EW7-0SIT or equivalent
GPS / GPSDO	P/N: u-blox ZOE-M8 GNSS SiP module NMEA sentences, PPS, and frequency-disciplining
GPS Antenna Input	U.FL antenna input, 3.3V bias for active GPS antenna, software enable/disable
Inertial Measurement Unit (IMU) Sensor	TDK / InvenSense ICM-20602 6-axis MotionTracking Device (3-axis gyroscope, 3-axis accelerometer) - Gyroscope sensitivity error: ±1% - Gyroscope noise: ±4 mdps/√Hz - Accelerometer noise: 100 µg/√Hz
Temperature Sensor	Texas Instruments TMP6131DECR Range: -40 deg C to +125 deg C (+/- 1 deg C typ) Resolution: 1 deg C
Component Temperature Rating	-30 deg C* to + 85 deg C **Operation down to -40 deg C is supported, though the TCVCXO will operate outside of the +/- 0.1 PPM accuracy specification.*

Table 5: *HW Spec*

HARDWARE INTERFACES

Sidekiq NV100 provides a variety of different hardware interfaces. Each of these hardware interfaces is shown in the annotated diagram and defined below.

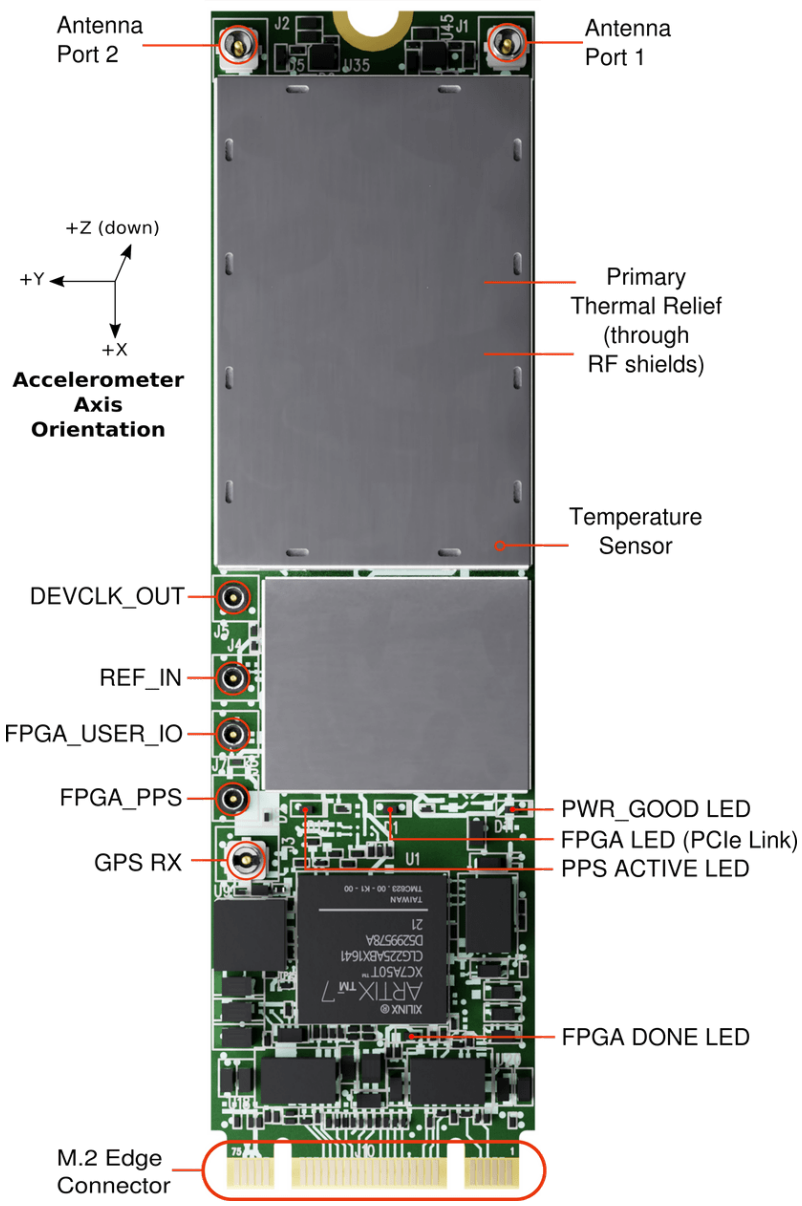

Figure 3: *Annotated diagram of Sidekiq NV100 hardware I/O interfaces*

ANTENNA PORT 1 (RXA1/RXB1/TXA1)

This RF interface is a U.FL jack connector **(J1)** that provides an RF input path for the RxA1 or RxB1 antenna ports, or an RF output path for the TxA1 antenna port, supports RF input frequencies up to 6 GHz. The maximum allowable RF input power level at this U.FL connector without causing damage is **+20dBm**.

The following libsidekiq software library handles can be mapped to this interface:

- RxA1 handle **skiq_rx_hdl_A1**
- RxB1 handle **skiq_rx_hdl_B1**
- TxA1 handle **skiq_tx_hdl_A1**

ANTENNA PORT 2 (TXB1/RXB1)

This RF interface is a U.FL jack connector **(J2)** that provides an RF output path for the TxB1 antenna port or an RF input path for the RxB1 antenna port, supports frequencies up to 6 GHz. The maximum allowable RF input power level at this U.FL connector without causing damage is **+20dBm**.

The following libsidekiq software library handles can be mapped to this interface:

- TxB1 handle **skiq_tx_hdl_B1**
- RxB1 handle **skiq_rx_hdl_B1**

This interface can also be switched to act as a second receive port, allowing a second RF connection for banded receive antennas or TDD support. The selection of either transmit or receive mode for this antenna port can be controlled via the libsidekiq software library.

Handle	RF Port [Fixed-Mode]	RF Port [TRX-Mode]
skiq_rx_hdl_A1	skiq_rf_port_J1	skiq_rf_port_J1
skiq_tx_hdl_A1	skiq_rf_port_J1	skiq_rf_port_J1
skiq_rx_hdl_B1	skiq_rf_port_J1 or skiq_rf_port_J2	skiq_rf_port_J2
skiq_tx_hdl_B1	skiq_rf_port_J2	skiq_rf_port_J2

Table 6: *RF Port Mapping*

GPS RX

This RF interface is a U.FL jack connector **(J3)** that provides an RF input path for the GPS antenna port (GNSS signal input). The maximum allowable RF input power level at the GPS RX U.FL connector without causing damage is **0 dBm**.

STATUS LEDS

The Sidekiq NV100 has 4 status LEDs with the following functions:

Status LED	ON	OFF
POWER GOOD	Sidekiq NV100 is powered up	Sidekiq NV100 is powered down
FPGA DONE	FPGA bitstream successfully loaded	FPGA bitstream is not loaded
GPS PPS	Pulses once per second when PPS source is present	PPS source is not present
FPGA (PCIe Link)	PCIe link has been established	PCIe link is not established

Table 7: *Status LEDs*

EXTERNAL PPS INPUT (FPGA PPS)

The External PPS Input interface is a W.FL jack connector **(J6)** that allows an external PPS signal to be brought into the on-board FPGA on Sidekiq NV100 for use in time synchronization as well as disciplining of the on-board reference clock. This signal is routed to the on-board FPGA through a 3.3V to 1.8V level shifter. A maximum recommended signal level of 3.3V can be applied to this input port. This PPS input is optional.

Note: Since this signal is ultimately routed directly to the on-board FPGA, it is possible to also use this signal as a general purpose input/output. Contact Epiq Solutions for details of alternate usage of this port.

EXTERNAL REFERENCE CLOCK INPUT (REF_IN)

The External Reference Clock Input interface is a W.FL jack connector **(J4)** that allows an external 10 or 40 MHz reference clock to be brought into Sidekiq NV100 and utilized instead of the default on-board 40 MHz TCVCXO. The selection between on-board TCVCXO and the external TCVCXO is controlled through the libsidekiq software API.

The electrical specification for this input signal is defined below.

Input Level	0.8 – 1.3 Vpp, 0 dBm max from 50 ohm source for 40 MHz 0.8 – 3.0 Vpp, +7 dBm max from 50 ohm source for 10 MHz
Input Impedance	AC-Coupled, high-impedance
Frequency	10 MHz or 40 MHz
Waveform	Square-wave
Connector Type	W.FL

Table 8: *Electrical specification for external reference clock input*

REFERENCE CLOCK OUTPUT (DEVCLK_OUT)

The External Reference Clock output interface is a W.FL jack connector **(J5)** that outputs the on-board 40 MHz TCVCXO reference clock.

The electrical specification for this output signal is defined below.

Output Level	~1.3 Vpp into high-Z load ~635 mVpp into 50 ohm load
Frequency	40 MHz
Waveform	Single-ended LVCMOS square wave output
Connector Type	W.FL

Table 9: *Electrical specification for reference clock output*

FPGA USER IO

The FPGA USER IO interface is a W.FL jack connector **(J7)** that provides access to a single FPGA GPIO pin. This allows for a digital single control signal to/from the FPGA to be accessed via a coaxial cable plugged into this connector. Common uses for this would be to control an external RF switch, an enable/disable line for an RF power amplifier, etc.

This signal is routed to the on-board FPGA (pin M18) through a 3.3V to 1.8V level shifter. A maximum recommended signal level of 3.3V can be applied to this port.

PRIMARY THERMAL RELIEF (RF SHIELD)

The RF shield (used to minimize the effects of RF noise entering the RF front end) serves as the primary thermal relief path for heat dissipation in the system. Underneath the shield, thermal gap pad material is used to transfer heat from components to the shield itself, yielding a minimal thermal resistance. If no air flow is available in the host system where Sidekiq NV100 is being integrated, it is highly recommended that the user provide a thermal dissipation path from this shield to a thermally conductive surface in the host system, such as a metal back plate or other metal housing. The use of thermal gap pad material can provide a flexible yet efficient thermal path between the RF shield and the host system.

In addition to the RF shield, the other primary component generating heat in Sidekiq NV100 is the Xilinx Artix 7 FPGA (which is located near the PCIe edge connector). If an end user is developing a thermal dissipation path for the RF shield, it is also recommended to include the FPGA in the thermal transfer path as well. Similar to the RF shield, use of a thermal gap pad material can be very effective in ensuring good thermal conductivity between this component and the host system.

TEMPERATURE & INERTIAL MEASUREMENT UNIT (IMU) SENSORS

The Sidekiq NV100 is equipped with a temperature sensor for monitoring on-board temperature and an IMU sensor for detecting orientation and tracking rotation or twist.

Please refer to the annotated NV100 diagram for the Sidekiq accelerometer axis orientation & temperature sensor location.

The libsidekiq software API provides access to these peripherals, *read_temp* and *read_imu* test applications are included are included for demonstrative use.

M.2 EDGE CONNECTOR

The M.2 Edge Connector is used to route various signals between the M.2 host system and the Sidekiq card. The Sidekiq NV100 card supports both Key B as well as Key M. A complete table enumerating the pins and their usage is shown in the table below.

Pin	M.2 Pin Name	Description
1	CONFIG_3	Unused (floating)
2	+3.3V	+3.3V supply
3	GND	Ground
4	+3.3V	+3.3V supply
5	GND	Ground
6	FC_POWER_OFF_N	Power down control
7	USB_DP	Unused (floating)
8	W_DISABLE1_N	Input only (FPGA pin J2), 3.3V tolerant
9	USB_DM	Unused (floating)
10	LED_1_N	Unused (floating)
11	GND	Ground
12	Key	N/A (Module B key)
13	Key	N/A (Module B key)
14	Key	N/A (Module B key)
15	Key	N/A (Module B key)
16	Key	N/A (Module B key)
17	Key	N/A (Module B key)
18	Key	N/A (Module B key)
19	Key	N/A (Module B key)
20	GPIO_5**	GPIO/FPGA_PPS input (FPGA pin N3), 1.8V signal, also connects to J6 RF port through a 3.3V level shifter
21	CONFIG_0	Unused (floating)
22	GPIO_6	MCS_IN (multi-chip sync input)
23	WoWWAN_N	Unused (floating)
24	GPIO_7	REFCLK_IN (device clock input)
25	DPR	Unused (floating)

26	W_DISABLE2_N	Unused (floating)
27	GND	Ground
28	GPIO_8*	GPIO (FPGA pin T18), 1.8V
29	PETN1	PCIe lane 1 host transmitter diff pair (data host->module)
30	UIM-RESET	JTAG TMS line for FPGA
31	PETP1	PCIe lane 1 host transmitter diff pair (data host->module)
32	UIM-CLK	JTAG TDO line for FPGA
33	GND	Ground
34	UIM-DATA	JTAG TDI line for FPGA
35	PERN1	PCIe lane 1 host receiver diff pair (data module->host)
36	UIM-PWR	JTAG TCK line for FPGA
37	PERP1	PCIe lane 1 host receiver diff pair (data module->host)
38	N/C	Unused (floating)
39	GND	Ground
40	GPIO_0/GNSS_SCL	TR_N_PROXY1 (FPGA pin L1), 1.8V
41	PETN0	PCIe lane 0 host transmitter diff pair (data host->module)
42	GPIO_1/GNSS_SDA	TR_N_PROXY2 (FPGA pin G3), 1.8V
43	PETP0	PCIe lane 0 host transmitter diff pair (data host->module)
44	GPIO_2/GNSS_IRQ*	GPIO2 (FPGA pin T17), 1.8V
45	GND	Ground
46	GPIO_3/GNSS_0*	GPIO3 (FPGA pin H2), 1.8V
47	PERN0	PCIe lane 0 host receiver diff pair (data module->host)
48	GPIO_4/GNSS_1	DEVCLK_IN
49	PERP0	PCIe lane 0 host receiver diff pair (data module->host)
50	PERST_N	PCIe reset
51	GND	Ground
52	CLKREQ_N	Clock Request, pulled low whenever Sidekiq NV100 is powered up
53	REFCLKN	PCIe reference clock negative leg of diff pair, from host
54	PEWAKE#	Unused (floating)
55	REFCLKP	PCIe reference clock positive leg of diff pair, from host
56	N/C	Unused (floating)
57	GND	Ground

58	N/C	Unused (floating)
59	Key	N/A (Module M key)
60	Key	N/A (Module M key)
61	Key	N/A (Module M key)
62	Key	N/A (Module M key)
63	Key	N/A (Module M key)
64	Key	N/A (Module M key)
65	Key	N/A (Module M key)
66	Key	N/A (Module M key)
67	RESET_N	1.8V I/O, hard reset when low
68	SUSCLK	Unused (floating)
69	CONFIG_1	Unused (floating)
70	3.3V	3.3V from host to power card
71	GND	Ground
72	3.3V	3.3V from host to power card
73	GND	Ground
74	3.3V	3.3V from host to power card
75	CONFIG_2	Pulled low through resistor to ground

Table 10: *Sidekiq NV100 edge connector signal descriptions*

** This indicates a GPIO pin that is preferred for use when interfacing to a custom host platform. These pins will receive priority in terms of GPIO backward compatibility if future variants of Sidekiq require changes to the GPIO allocation.*

*** This GPIO pin is preferred for receiving a PPS input signal from the host platform.*

BASIC USAGE IN A HOST SYSTEM

HOST SYSTEM COMPATIBILITY

From a hardware perspective, Sidekiq NV100 is mechanically and electrically compatible with host systems that provide a standards-compliant M.2 2280 Key B+M card slot. These slots are typically used for PCIe-based NVMe® solid state drives (SSDs). Laptops and other embedded systems generally have multiple of these memory slots and in this case the Sidekiq NV100 can be accommodated along with SSDs.

USB/PCIE SIGNAL AVAILABILITY IN HOST PLATFORM

The Sidekiq NV100 is designed solely with a PCIe interface. USB is not present in standard M.2 2280 SSD slots and not included in the standard edge connector profile.

BIOS COMPATIBILITY

Different host systems enforce different rules regarding which M.2 cards are considered to be compatible with their platform. Generally these rules are for M.2 cards that are connecting on USB, we have not seen limitations based on PCI IDs. It is still recommended that the end user verify whether or not their intended host system imposes any limitations regarding compatible cards.

OPERATING SYSTEM COMPATIBILITY

Windows 10 is currently supported.

Various Linux kernel versions have been tested starting at version 3.0. Sidekiq has been tested both in x86-based Linux systems, Ubuntu & CentOS distributions are preferred, as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported. Please contact Epiq Solutions for details.

For customers interested in doing a custom build of the Sidekiq PCIe device driver for their host platform, a license for the source code for this device driver is also available separately. Please contact Epiq Solutions for details.

FPGA REPROGRAMMING OPTIONS

The FPGA bitstream can also be fully reconfigured at run-time with a new bitstream from the host system via PCIe interface or from any one of the six on-board flash configuration slots available. This allows new FPGA bitstreams to be loaded into the FPGA using the PCIe interface or directly

from the on-board flash. Complete reconfiguration is followed by an FPGA reset operation to re-load the bitstream from flash, during which the device will disappear from the PCIe bus.

Multiple FPGA bitstreams can be stored in flash and the FPGA can be configured from any slot that contains a valid bitstream. Each flash configuration slot contains the FPGA bitstream and has 64 bits of metadata associated with the slot. The user may use this metadata to create a mapping between the stored bitstream and its intended purpose. For example, the user can store an abbreviated hash of the bitstream in the metadata so that a full dump of the flash contents is not necessary when verifying what bitstream is stored in the config slot.

RF INTERFACES

Some host systems that support M.2 2280, such as laptops, come pre-wired with antennas already integrated into the host system. The range of RF frequencies supported by these antennas, as well as the gain of the antennas, will be platform specific. Typically, these internal antennas have support for cellular frequencies (700 MHz to 1 GHz, and 1700 MHz to 2.1 GHz) as well as Wi-Fi frequencies (2.4 GHz and 5.9 GHz), but it is up to the user to validate the performance of the antenna solution.

SYSTEM INTERFACE

The Sidekiq NV100 is designed to interface to a host system through insertion into a PCIe-based M.2 2280 key B or M socket, commonly used for NVMe® solid state drives (SSD).

Note: Sidekiq NV100 should never be inserted into or removed from a host system with power applied to the host system. This could permanently damage the card or the host system.

PROPER DETECTION OF SIDEKIQ NV100 IN A WINDOWS HOST SYSTEM

A properly configured Windows host system (with the necessary device driver loaded) will allow Sidekiq NV100 to enumerate on the PCIe bus.

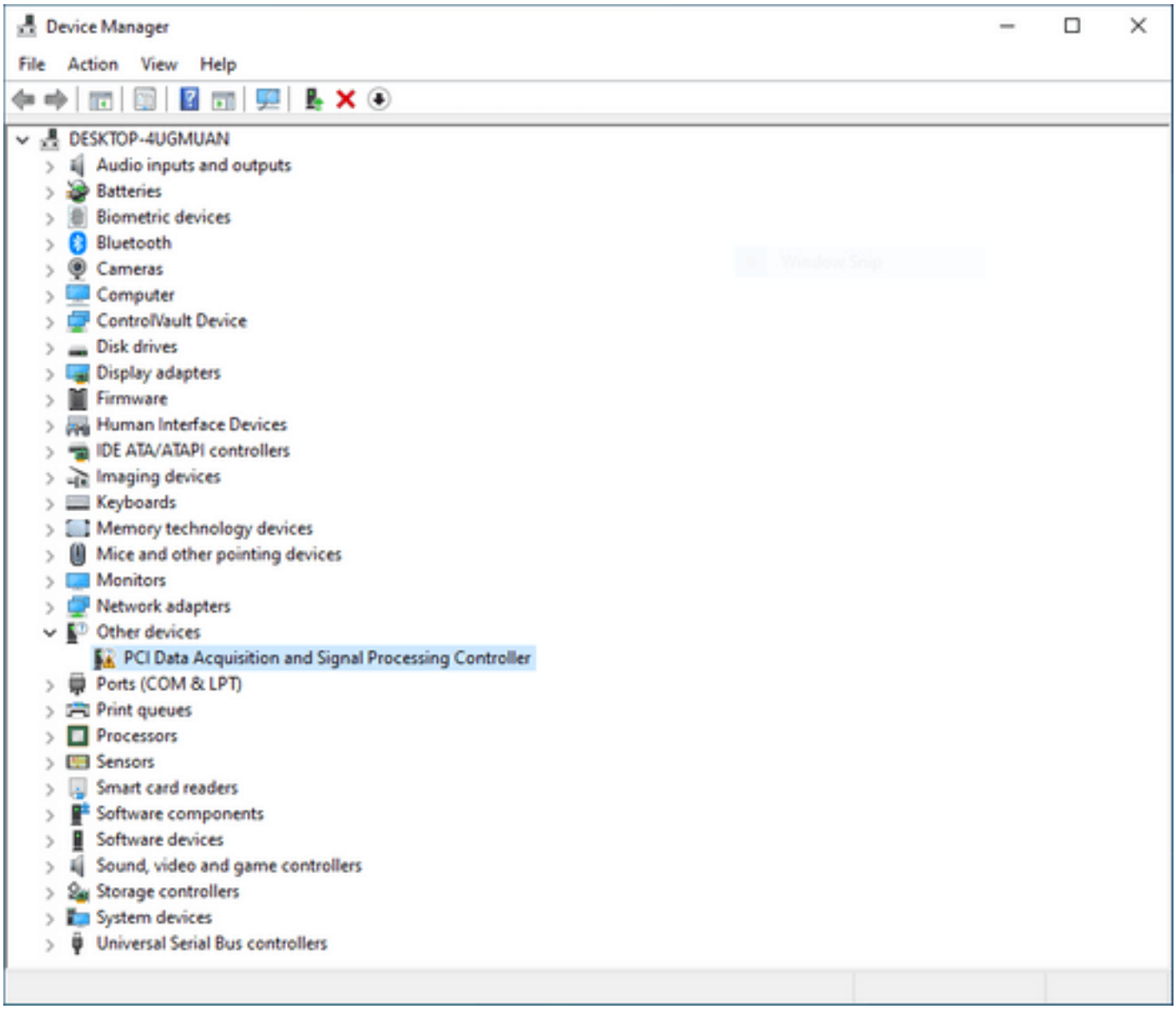

Figure 4: *Detection of Sidekiq in Windows 10*

Please refer to the Windows Sidekiq Development section of the Sidekiq Software Development Manual for additional information. The Sidekiq Software Development manual is available through the support site: https://support.epiqsolutions.com

PROPER DETECTION OF SIDEKIQ NV100 IN A LINUX HOST SYSTEM

A properly configured Linux host system (with the necessary device drivers loaded) will allow Sidekiq NV100 to enumerate on the PCIe bus. The enumeration on the PCIe bus can be verified by executing the command "*lspci*" to confirm the presence of Sidekiq. The execution of the "*lspci*"

command from the terminal will provide output similar to the following when Sidekiq is detected and shows up as "**Signal processing controller: Device 19aa:2280 (rev 04)**":

```
...
00:00.0 Host bridge: Intel Corporation Xeon E3-1200 v5/E3-1500 v5/6th Gen Core
Processor Host Bridge/DRAM Registers (rev 07)
00:01.0 PCI bridge: Intel Corporation Xeon E3-1200 v5/E3-1500 v5/6th Gen Core
Processor PCIe Controller (x16) (rev 07)
00:02.0 VGA compatible controller: Intel Corporation HD Graphics 530 (rev 06)
06:02.0 PCI bridge: Intel Corporation JHL6340 Thunderbolt 3 Bridge (C step) [Alpine
Ridge 2C 2016] (rev 02)
07:00.0 System peripheral: Intel Corporation JHL6340 Thunderbolt 3 NHI (C step)
[Alpine Ridge 2C 2016] (rev 02)
08:00.0 PCI bridge: Intel Corporation JHL6340 Thunderbolt 3 Bridge (C step) [Alpine
Ridge 2C 2016] (rev 02)
09:01.0 PCI bridge: Intel Corporation JHL6340 Thunderbolt 3 Bridge (C step) [Alpine
Ridge 2C 2016] (rev 02)
0a:00.0 Signal processing controller: Device 19aa:2280 (rev 04)
```

POWER CONSUMPTION

The power consumption of Sidekiq NV100 varies depending on the configuration and application of the card. Nominal tolerance of the 3.3V rail is +/-9%.

The table below lists the power consumption with the stock Sidekiq NV100 FPGA reference design (v3.16.0) and libsidekiq v4.17.0 under different operating conditions. The measured card temperature was 57 deg C during testing.

Test Scenario	Power (in Watts)
Idle, not initialized,	2.67 W
Idle, libsidekiq initialized with *version_test --full*	2.69 W
rx_benchmark test app: *where --handle=a1 is single channel and --handle=a1,b1 is two channel receive* ./rx_benchmark -r 0.541667e6 --handle=a1	3.86 W
./rx_benchmark -r 0.541667e6 --handle=a1,b1	4.22 W
./rx_benchmark -r 5.6e6 --handle=a1	4.15 W
./rx_benchmark -r 5.6e6 --handle=a1,b1	4.52 W
./rx_benchmark -r 16e6 --handle=a1	4.25 W
./rx_benchmark -r 16e6 --handle=a1,b1	4.62 W
./rx_benchmark -r 30.72e6 --handle=a1	4.31 W
./rx_benchmark -r 30.72e6 --handle=a1,b1	4.71 W
./rx_benchmark -r 61.44e6 --handle=a1	4.43 W
./rx_benchmark -r 61.44e6 --handle=a1,b1	4.92 W

rx_samples test app: *where --handle=a1 is single channel and --handle=all is two channel receive* Rx @ 850 MHz / 0.541667 Msamples/sec, GPS searching, no antenna connected: ./rx_samples -r 30.72e6 -b 50e6 -f 850e6 --handle=a1 -d /tmp/rx	4.37 W
Rx @ 850 MHz / 30.72 Msamples/sec, GPS searching, no antenna connected ./rx_samples -r 30.72e6 -b 50e6 -f 850e6 --handle=all -d /tmp/rx	4.78 W
tx_benchmark test app: ./tx_benchmark -r 0.541667e6 --threads=4 --block-size=16380	4.45 W
./tx_benchmark -r 5.6e6 --threads=4 --block-size=16380	4.83 W
./tx_benchmark -r 16e6 --threads=4 --block-size=16380	4.99 W
./tx_benchmark -r 30.72e6 --threads=4 --block-size=16380	5.01 W
./tx_benchmark -r 61.44e6 --threads=4 --block-size=16380	5.13 W
xcv_benchmark test app: ./xcv_benchmark -r 0.541667e6 --threads=4 --block-size=16380	4.22 W
./xcv_benchmark -r 5.6e6 --threads=4 --block-size=16380	4.59 W
./xcv_benchmark -r 16e6 --threads=4 --block-size=16380	4.64 W
./xcv_benchmark -r 30.72e6 --threads=4 --block-size=16380	4.74 W

Table 11: *Example power consumption estimates for Sidekiq NV100*

GPS POWER CONSUMPTION (TBD)

State	Current	Power (3.25V) in Watts
GPS searching/antenna on	TBD	TBD
GPS searching/antenna off	TBD	TBD
Antenna bias	TBD	TBD
GPS tracking/antenna on	TBD	TBD

Table 12: *GPS Power Consumption*

Note that the antenna bias power requirement is not included in the overall Sidekiq NV100 test results. Power will depend on the particular active antenna used. The (TBD) mA shown above is typical for most modern antennas, but some older antennas may require several times more power.

THERMAL DISSIPATION

Effective use of Sidekiq NV100 in a system also requires consideration of an appropriate thermal dissipation solution. Since Sidekiq NV100 can be integrated into a variety of different host systems with different thermal profiles (i.e., forced air, natural convection, etc), the end user is required to

perform their own system analysis to determine what level of thermal dissipation is appropriate for their use-case. Sidekiq NV100 uses components that are rated for operation to +85 deg C, and thus the end user must ensure that the temperature reported by the on-board temperature sensor does not exceed +85 deg C. **Exceeding the maximum rated temperature of +85 deg C may damage the Sidekiq NV100 card and/or accelerate failure of the card.**

As discussed in the Primary Thermal Relief (RF Shield) section, both the RF shield as well as the FPGA are the two primary sources of heat requiring thermal dissipation. It is highly recommended that a thermal transfer solution, such as gap pad material, be used to provide a thermal dissipation path between the RF shield/FPGA and an external conduction surface in the host system. With adequate thermal transfer to the host system, it is common for Sidekiq NV100 to report steady state board temperatures in the range of 55 deg C to 60 deg C while fully operational. Note: The actual temperature range achievable in a given system may vary substantially depending on a number of factors, including the function of the RF receiver and/or the RF transmitter, the A/D and D/A sample rates, customizations done to the FPGA, and others. Again, it is strongly recommended that a thorough system evaluation be performed by the customer to fully characterize the thermal profile of Sidekiq NV100 in their system.

INTERNAL/EXTERNAL REFERENCE CLOCK OPTIONS

Sidekiq NV100 supports options to use either an internal or external reference clock. The internal reference clock is a SiTime SiT5356 high stability MEMS oscillator. This oscillator has 0.1ppm frequency stability over temperature with +/- 6ppm tuning range. The GPS receiver module can also be used to lock the Sidekiq NV100's internal oscillator to GPS timing/frequency.

The external reference clock can be either a 10 MHz or 40 MHz clock.

Regardless of which clock source is selected, this clock serves as the reference for both the RF front end as well as the digital processing blocks in the FPGA. The selection of whether the Sidekiq NV100 uses the internal 40 MHz reference clock or an external 10 or 40 MHz reference clock is stored as a configuration parameter in EEPROM on the card. This parameter is read at power-up, and is used to configure how the card should operate.

If the Sidekiq NV100 is configured to use an external reference clock, but no external reference clock is provided via the W.FL connector, RF performance will be undefined.

For cases where a customer would like to switch between internal and external reference clock options, a *ref_clock* software test application is provided to update the EEPROM configuration settings. The Sidekiq NV100 also provides it's 40 MHz reference clock output to a W.FL connector at a level suitable for driving other Sidekiq cards (MiniPCIe, M.2, Stretch, or NV100). Please consult with Epiq for optimum clock tree layouts for a given multi-radio architecture.

Note, run-time reference clock source management and control support for Sidekiq NV100 is available with libsidekiq v4.17.0 or later using *skiq_write_ref_clock_select()* API function.

GPS DISCIPLINED OSCILLATOR (GPSDO)

Sidekiq NV100 features hardware to support a GPS disciplined oscillator. The key components are the GPS receiver module with a 1 pulse per second (PPS) output and a voltage control oscillator (VCO). The on-board GPS / GNSS receiver module provides GPS timing as well as positioning and navigational data. The GPS receiver module, u-blox ZOE-M8, is a miniature multi-channel GPS/QZSS, GLONASS, GALILEO, and BEIDOU receiver that continuously tracks all satellites in view, providing real-time positioning data in industry standard NMEA format.

The Sidekiq NV100 also provides a W.FL connector with the GPS receiver's pulse-per-second (PPS) signal for synchronizing additional radio modules.

The GPS Disciplined Oscillator (GPSDO) functionality can be enabled using the libsidekiq API *skiq_gpsdo_enable()* function. When a GPS fix has been obtained by the on-board GPS, the FPGA uses the 1PPS signal to increase the accuracy of the radio's TCVCXO by automatically adjusting the DAC warp voltage. If no GPS fix can be obtained or is lost, the DAC warp voltage is kept at its current value; if no GPS fix is available on startup, the warp voltage is kept at its factory calibrated default value. As the FPGA is now in control of the warp voltage, this prevents its manual adjustment through the API.

GPSDO PERFORMANCE

The GPSDO on Sidekiq NV100 was tested under the following conditions:

- Ambient temperature was approximately 25 C. The NV100 had a heat sink attached but no airflow was directed at it (natural convection only)
- A rooftop GPS antenna and distribution system was used to provide a high-quality GPS signal to the NV100
- The GPSDO was given about 60 minutes to lock and converge the tracking loop.
- Frequency measurements on the 40 MHz disciplined oscillator were made for 12 hours at a 10 Hz
- Tested with Keysight 53230A frequency counter

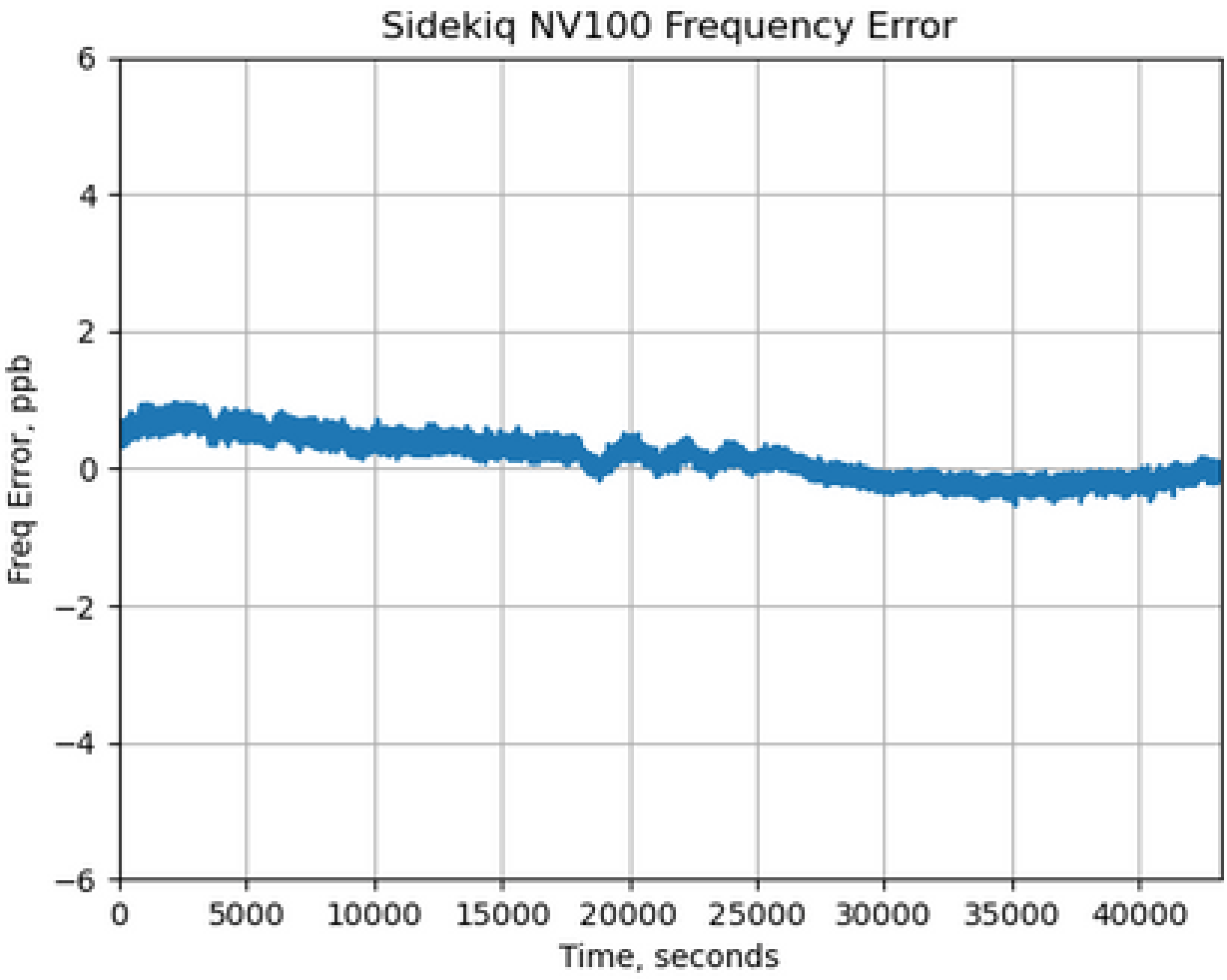

Figure 5: *Frequency Error vs Time*

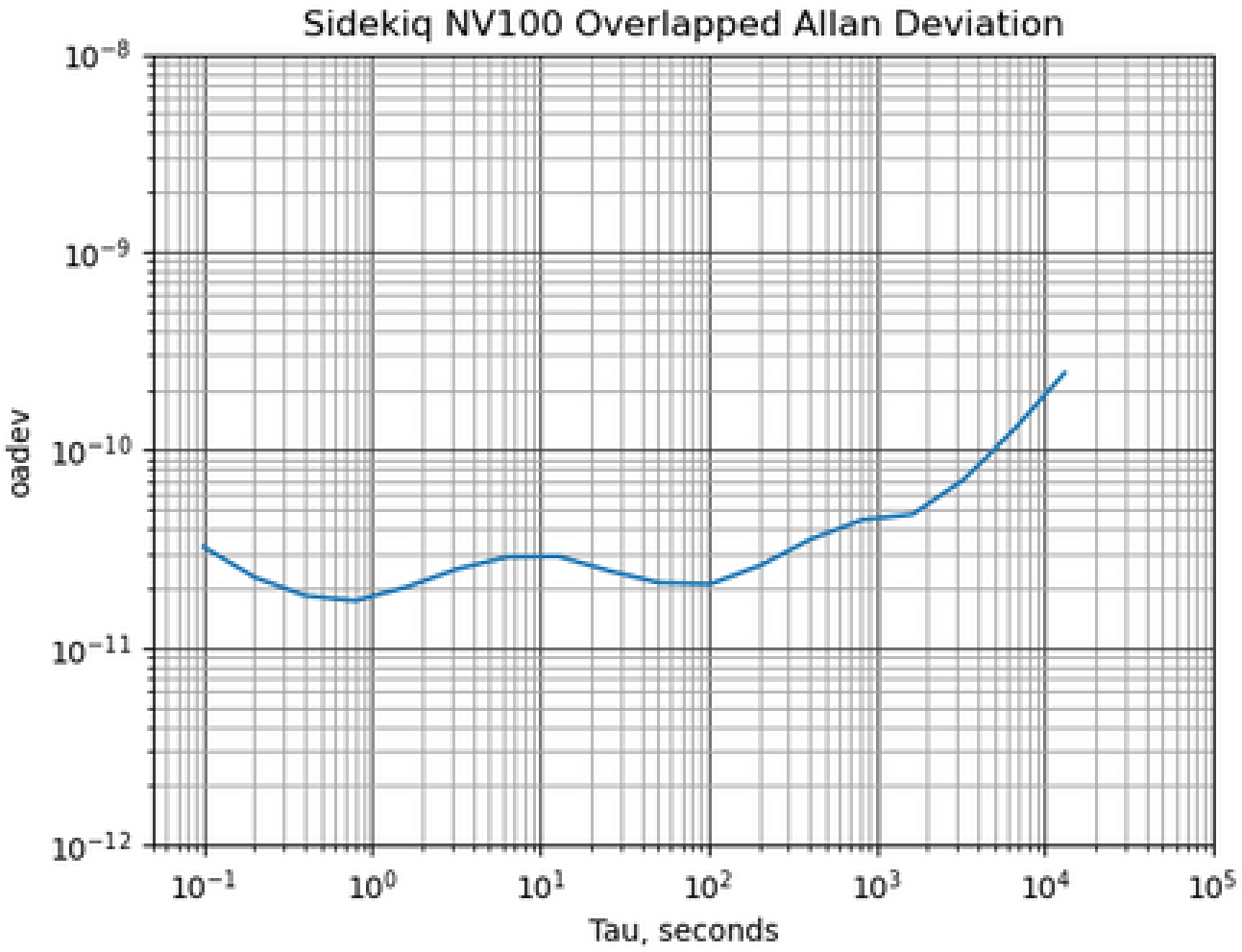

Figure 6: *Allan Deviation*

GPS / UART FUNCTIONALITY IN LINUX HOST SYSTEM

SIDEKIQ NV100 GPS SYSFS

Control and status monitoring of Sidekiq NV100's on-board GPS is provided through several sysfs entries on the host system. When both the *sidekiq_uart.ko* kernel module and the *dmadriver.ko* (v5.3.0 or later) kernel module are loaded, several sysfs entries are available in `/sys/fs/skiq_gps/<card>` where `<card>` is the Sidekiq NV100's card index.

These entries are accessible from any application, whether it uses libsidekiq or not. A short summary of the available entries as of v0.0.2 of *sidekiq_gps* are as follows:

Entry	Description	State
ant_bias_en	Enables or disables antenna bias	(1) enabled / (0) disabled
has_fix	GPS Fix Status	(1) GPS has fix / (0) GPS does not have fix
power_en_n	Power to GPS module	(1) disabled / (0) enabled
reset	Control the RESET line to the GPS module	(1) holds the device in reset / (0) allows the device to run

Table 13: *Useful sysfs entries*

Linux sysfs GPS Control Examples

To read the GPS sysfs entries:

```
$ cd /sys/fs/skiq_gps/0/

$ ll
total 0
drwxr-xr-x 2 root root    0 Oct  8 12:49 ./
drwxr-xr-x 3 root root    0 Oct  8 12:49 ../
-rw-r--r-- 1 root root 4096 Oct  8 12:49 ant_bias_en
-r--r--r-- 1 root root 4096 Oct  8 12:49 has_fix
-rw-r--r-- 1 root root 4096 Oct  8 12:49 power_en_n
-rw-r--r-- 1 root root 4096 Oct  8 12:49 reset

$ tail -n1 *
==> ant_bias_en <==
0

==> has_fix <==
0

==> power_en_n <==
0

==> reset <==
0
```

To enable the GPS antenna bias:

```
$ cd /sys/fs/skiq_gps/0
$ echo 1 | sudo tee ant_bias_en
```

Verify GPS antenna bias is enabled and GPS fix:

```
$ ll
total 0
drwxr-xr-x 2 root root    0 Oct  8 12:49 ./
drwxr-xr-x 3 root root    0 Oct  8 12:49 ../
-rw-r--r-- 1 root root 4096 Oct  8 12:49 ant_bias_en
-r--r--r-- 1 root root 4096 Oct  8 12:49 has_fix
-rw-r--r-- 1 root root 4096 Oct  8 12:49 power_en_n
-rw-r--r-- 1 root root 4096 Oct  8 12:49 reset

$ tail -n1 *
==> ant_bias_en <==
1

==> has_fix <==
1

==> power_en_n <==
0

==> reset <==
0
```

SIDEKIQ NV100 GPS UART

The Sidekiq NV100's on-board GPS can provide NMEA-0183 messages through a UART device on the host system. When both the *sidekiq_uart.ko* kernel module and the *dmadriver.ko* (v5.3.0 or later) kernel module are loaded, a UART character device file is available as `/dev/ttySKIQ_UART<card>` where `<card>` is the NV100's card index. This device file may be used directly in any application (whether it uses libsidekiq or not) to receive NMEA-0183 messages.

This device file may also be used in conjunction with *gpsd* and *gpsmon*.

```
$ gpsmon 127.0.0.1:2947
```

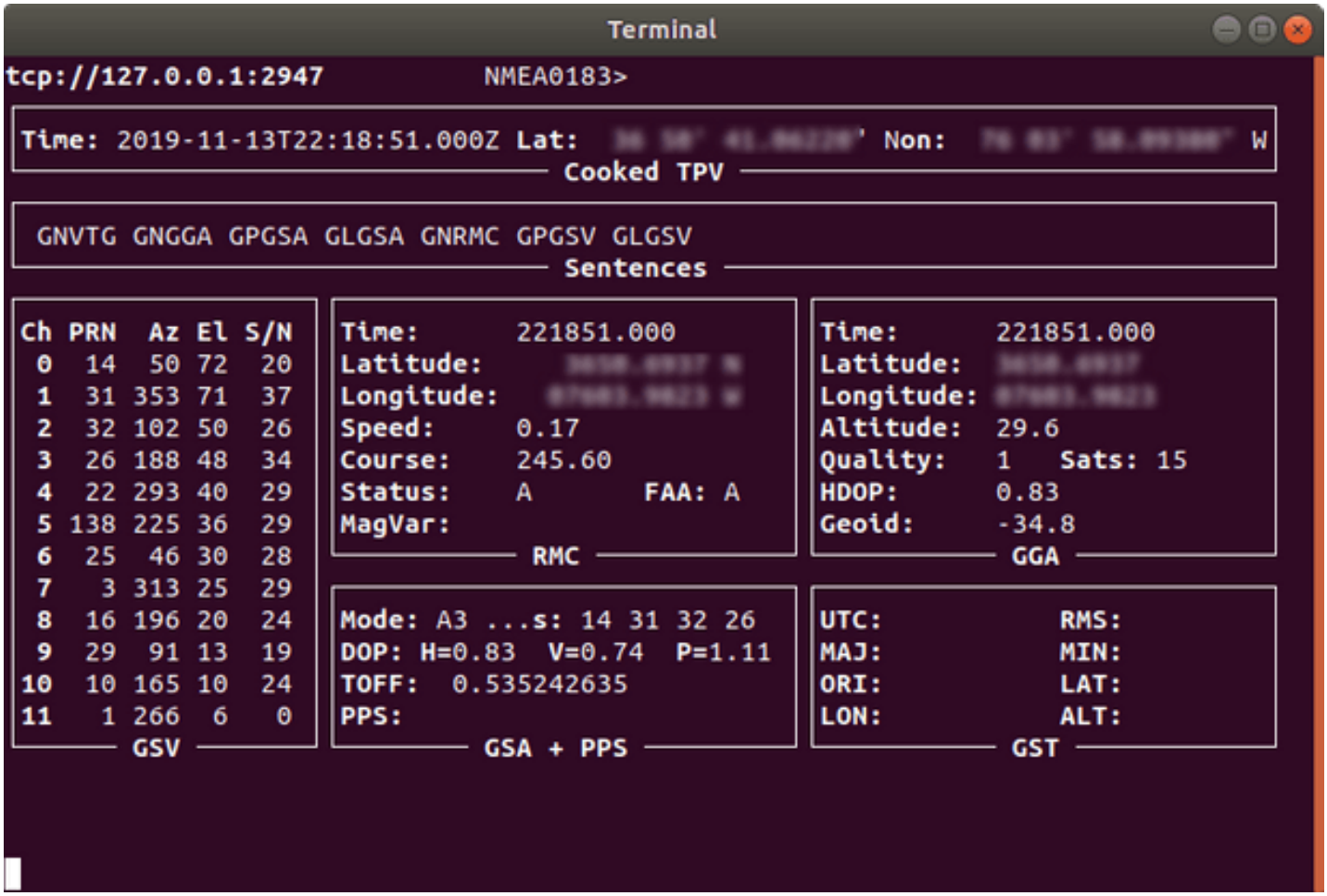

Figure 7: *GPSMON Example*

Note, Linux distros such as Ubuntu 20.04 have AppArmor (Mandatory Access Control (MAC) system) which is a kernel (LSM) enhancement to confine programs to a limited set of resources. If this feature is enabled/enforcing, customers using GPSD service daemon will need to add the SKIQ_UART device to /etc/apparmor.d/usr.sbin.gpsd `/dev/tty{,S,**SKIQ_UART**,USB,AMA,ACM}[0-9]* rw,`

GPS / UART FUNCTIONALITY IN WINDOWS HOST SYSTEM

Windows support for this feature will be available in a future software release.

SUPPORT FOR HOST SYSTEM SLEEP/HIBERNATION

Some host systems that have a “sleep mode” or “hibernation” mode where power is no longer applied to the M.2 slot while in this state. Sidekiq does *not* currently have proper support to handle these transitions, since the FPGA bitstream would be lost during this transition. Thus, if the host system enters into a sleep/hibernation state, it should be assumed that the Sidekiq NV100 card will likely need to undergo a complete reboot in order to fully use all of the features of the card again. For example, if a Sidekiq NV100 card is installed in a laptop with power savings mode enabled each time the laptop lid closes, proper Sidekiq operation is not guaranteed after the laptop lid is reopened.

DEBUGGING THE SIDEKIQ NV100

JTAG ACCESS ON SIDEKIQ NV100

The Xilinx Artix 7 XC7A50T FPGA utilized on Sidekiq NV100 provides a JTAG interface that can be accessed and utilized during the development of custom logic/processing modules targeting the FPGA. However, due to physical size constraints, there is no space available on Sidekiq NV100 for a standard JTAG interface. Thus, the JTAG interface signals are routed to the M.2 edge connector. The Sidekiq NV100 NUC or the Sidekiq NV100 JTAG Fixture can be used for accessing the JTAG signals via a standard FPGA JTAG programmer / debugger, such as the Xilinx 14-pin connector or the Digilent HS2 and HS3 pods with a compatible connector. The Sidekiq NV100 JTAG Fixture below shows the Sidekiq NV100 installed on the breakout board. Note: No additional power source is required for the breakout board, as it is derived from the host system, through the 3.3V interface provided by the M.2 connector.

SIDEKIQ NV100 JTAG FIXTURE USAGE NOTES

The following section provides usage notes for the Sidekiq NV100 JTAG Fixture.

- Details of using Xilinx tools to program and debug FPGA bitstreams with Sidekiq NV100 can be found in the Sidekiq NV100 FPGA Developer's Manual
- The Sidekiq NV100 JTAG Fixture is powered through the USB-C / TB3 interface. No additional power supply is required for the JTAG Fixture.
- The JTAG Fixture is a separate standalone unit that includes a Sidekiq NV100. Please take the appropriate precautions when handling static sensitive electronics, including working on a grounded anti-static mat and using a grounded anti-static wrist band.

Figure 8: *Sidekiq NV100 JTAG Fixture*

U.FL Connector	GPIO	Description
J4	GPIO_4	DEVCLK_IN
J5	GPIO_7	REFCLK_IN
J6	GPIO_6	MCS_IN
J7	GPIO_5	FPGA_PPS

Table 14: *Sidekiq NV100 JTAG Fixture U.FL Connectors*

Description	Pin	Pin	Description
V1P8	1	2	GPIO_0
GPIO_1	3	4	GPIO_2
GPIO_3	5	6	GPIO_4
FPGA_PPS	7	8	GPIO_6
GPIO_8	9	10	GND

Table 15: *Sidekiq NV100 JTAG Fixture GPIO Header (J8)*

Description	Pin	Pin	Description
NC	1	2	VREF (V1.8)
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	NC
PGND	13	14	HALT (NC)

Table 16: *Sidekiq NV100 JTAG Fixture Xilinx Header (J1)*

USB-C / TB3: Thunderbolt 3 over locking USB-C connector, provides both power and data transport (PCIe x2)

SIDEKIQ NV100 JTAG FIXTURE THUNDERBOLT3 (TB3) SETUP

1. Remove and verify that all the package contents are present as outlined in the Sidekiq NV100 paperwork.
2. Connect the NV100 JTAG fixture's TB3 port to the host computer's TB3 port with the provided TB3 cable.
3. If you are using the GPS, connect the GPS antenna to NV100 JTAG fixture's GPS RX port SMA.
4. Connect an antenna or RF source to RX and antenna or spectrum analyzer to TX before using any of the test applications.
5. Powering on the computer will also power on the NV100 JTAG fixture.
6. Enter computer’s BIOS Setup screen, Dell uses [F2] for example, to verify that Thunderbolt 3 support is enabled.

   Dell BIOS Settings Example:

   - Settings → System Configuration → Thunderbolt Adapter Configuration:
   - Enable Thunderbolt Technology Support
   - Enable Thunderbolt Adapter
   - Enable Thunderbolt Adapter Pre-boot Modules
   - Security level - No security
7. Refer to the Proper Detection of Sidekiq NV100 in a Windows Host System or Linux Host System section to verify that the Sidekiq NV100 is seen over PCIe by the host.
8. If Sidekiq NV100 is not seen over PCIe, power everything down and repeat the steps above, if the PCIe interface is still not detected, please contact Epiq Solutions support for further assistance.

SIDEKIQ NV100 NUC PLATFORM DEVELOPMENT KIT (PDK)

SIDEKIQ NV100 NUC PDK OVERVIEW

The Sidekiq NV100 NUC PDK includes one Sidekiq NV100 card hosted on an Intel NUC11TNHi5/i7 (or later) Mini PC NUC system.

The Sidekiq NV100 NUC PDK is pre-loaded with Epiq Solutions' libsidekiq API, test applications, ERA (Spectrum Analyzer), and GNU Radio with gr-sidekiq. All support-related questions, product documentation, software, and FPGA reference designs are managed through Epiq Solutions' private web-based support forum available at: https://support.epiqsolutions.com

Figure 9: *Sidekiq NV100 NUC hardware I/O interfaces*

SIDEKIQ NV100 NUC PDK SETUP

After you have removed all of the package contents, setup the system as follows:

1. Connect a USB keyboard and mouse to available USB ports; HDMI monitor to HDMI port; a network cable to the RJ45 port; and the DC power supply cable from the provided DC power brick.
2. Connect an antenna or RF source to the TRx1 SMA connector shown above before using any of the test applications or ERA; for more details, see “Sidekiq NV100 NUC RF Ports” below.
3. Power on the NUC, the computer monitor will indicate that it is starting up Ubuntu Linux and then it will show a login page.
4. Log into Ubuntu with the user credentials:

   Username: **sidekiq** Password: **sidekiq**

Included Applications

Several applications are included with the PDK in order to help you test and verify your setup, such as our standard Sidekiq command-line test applications, GNU Radio, and ERA, our spectrum analyzer.

Libsidekiq Test Applications are located in `/home/sidekiq/sidekiq_image_current/test_apps`

Launch a terminal window from Dash (search for “Terminal”) or by pressing Ctrl-Alt-T and then goto test_apps directory:

```
cd /home/sidekiq/sidekiq_image_current/test_apps/
```

A user can scan the system for Sidekiq cards, displaying version information for one or all card(s) upon detection by running the *version_test* application by executing the command:

```
./version_test
```

The application should return results that look something like the following:

```
**********************************************************
* Sidekiq Card 0
  Card
    accelerometer present: true
    part type: NV100
    part info: ES035201-C0-00
    serial: XXXX
    xport: PCIe
    GPSDO: available and present
  FPGA
    version: 3.16.0
    git hash: 0x00217183
    build date (yymmddhh): 21082618
    baseline git hash: 0x00217183
    tx fifo size: 16k samples
  RF
    reference clock: internal
    reference clock frequency: 40000000 Hz
```

Raw I/Q Capture

A user can perform an RF capture of I/Q samples using the default configuration by executing the *rx_samples* application as follows:

```
./rx_samples -c 0 --handle=A1 -r 22e6 -b 16e6 -f 1e9 --words=250000 -d /tmp/out
```

This command will save I/Q samples to a file named */tmp/out.a1* using values for 22 Msps sample rate, 16 MHz channel bandwidth, 1 GHz tune frequency. The data is stored in the file as 16-bit I/Q pairs with ‘I’ samples stored in the upper 16-bits of each word, and ‘Q’ samples stored in the lower 16-bits of each word. Additional available options are described by executing:

```
./rx_samples -h
```

ERA - Epiq RF Analyzer

EPIQ RF Analyzer (ERA) is installed on the Sidekiq NUC PDK. ERA is an application that controls an Epiq radio and provides a real time view of spectrum, radio frequency, sample rate, and filtering configuration.

The ERA User’s manual is available on support forum: https://support.epiqsolutions.com/viewforum.php?f=358 and provides instructions on the features and operation of ERA; some of these features described in the manual require the purchase of an ERA Pro license.

Running ERA

To run ERA, choose the Ubuntu icon in the top-left corner of the desktop and type “ERA”; the icon should appear in the “Applications” section.

SIDEKIQ NV100 NUC RF PORTS

NUC SMA Label	Sidekiq NV100 RF Ports
REF	(REF_IN) External REF Clock Input (10 or 40 MHz)
PPS	FPGA_PPS
GPS	GPS RX
TRx1	Antenna Port 1 (RX1/RX2/TX1)
TRx2	Antenna Port 2 (RX2/TX2)

Table 17: *Sidekiq NV100 NUC RF Ports*

SIDEKIQ NV100 NUC GPIO CONNECTOR

The GPIO connector provides access to monitoring the power supply voltage and current to the M.2 socket as well as providing access to lines used for digital I/O on the Sidekiq NV100. The ability to use a pin as GPIO depends on the loaded FPGA. The connector is a 2x8 header, 0.1" pin spacing, 0.025" square pins (standard size & spacing), Harwin P/N M20-9740846.

Function	Pin	Pin	Function
V_SENSE	1	2	GND
I_SENSE	3	4	GND
W_DISABLE M.2 pin 8	5	6	GND
GPIO_7 (REFCLK_IN) M.2 pin 24	7	8	GND
GPIO_0 M.2 pin 40	9	10	GPIO_1 M.2 pin 42
GPIO_2 M.2 pin 44	11	12	GPIO_3 M.2 pin 46
GPIO_5 (FPGA_PPS, input only) M.2 pin 20	13	14	GPIO_4 (DEVCLK_IN) M.2 pin 48
GPIO_6 (MCS_IN) M.2 pin 22	15	16	GND

Table 18: *Sidekiq NV100 NUC GPIO Connector*

V_SENSE: the voltage at the Sidekiq card. Nominally 3.3V

I_SENSE: outputs a voltage proportional to current in volts/amp, i.e., 0.4 V means the Sidekiq card is drawing 400mA

SIDEKIQ NV100 NUC JTAG CONNECTOR

The JTAG connector is a Samtec P/N STMM-107-02-G-D-RA. It will allow the standard Xilinx 14-pin JTAG cable to be attached.

Description	Pin	Pin	Description
NC	1	2	VREF*
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	NC
GND	13	14	NC

Table 19: *Sidekiq NV100 NUC JTAG Connector*

VREF* is a 1.8V output and establishes the required I/O voltage level for the JTAG adapter.

ACCESSING SIDEKIQ NV100 NUC JTAG CONNECTOR

For customers adding their own custom FPGA blocks in the “user_app” area of the Sidekiq NV100 reference design, it can often be useful to access JTAG to monitor signals in the FPGA through Xilinx's Chipscope software. The Sidekiq NV100 NUC PDK provides access to the Sidekiq’s JTAG port of the Xilinx Artix XC7A50T FPGA through a 2x7 header shown above. A standard Xilinx JTAG USB platform cable, such as the HW-USB-II-G, can be utilized to access JTAG on the FPGA.

Note: the default reference design does not have Chipscope ILA instantiated and users will need to create a Chipscope ILA core through the GUI ip core generator inside Vivado when building their custom design.

SIDEKIQ NV100 FLASH RECOVERY

The Flash device is Micron MT25QU128ABA1EW7-0SIT or equivalent.

If the Sidekiq's flash contents become corrupted (standard bitstream and golden image) and the PCIe-interface cannot be detected by the OS with lspci, you can recover the flash using Vivado and

a JTAG module following these steps:

1. Power up the Sidekiq NV100
2. Remove the Sidekiq Drivers (if loaded)

```
$ sudo rmmod sidekiq_gps; sudo rmmod sidekiq_uart; sudo rmmod pci_manager; sudo rmmod
dmadriver; sudo rmmod skiq_platform_device
```

3. Remove Sidekiq NV100 from the PCI bus (if detected)

```
$ lspci -d 19aa:
0a:00.0 Signal processing controller: Device 19aa:2280 (rev 04)
$ echo 1 | sudo tee /sys/bus/pci/devices/0000:0a:00.0/remove
```

'0000:0a:00.0' will change depending on where on the PCI bus NV100 is located

4. Program the FPGA using Vivado using an older Sidekiq NV100 bitstream such as `sidekiq_image_nv100_xport_pcie_3.16.0.bin` (or later) from Sidekiq SDK v4.17.0 (or later) located on the support forum: https://support.epiqsolutions.com/viewforum.php?f=148t/

   Download and extract, the bitstream can be found in the install directory `/home/sidekiq/sidekiq_image_v4.17.0_<timestamp>/fpga`(or later)

   The sidekiq_hardware_updater will detect an this older version and update the flash with the latest and greatest (v3.xx.x) for example, in step 8 below.

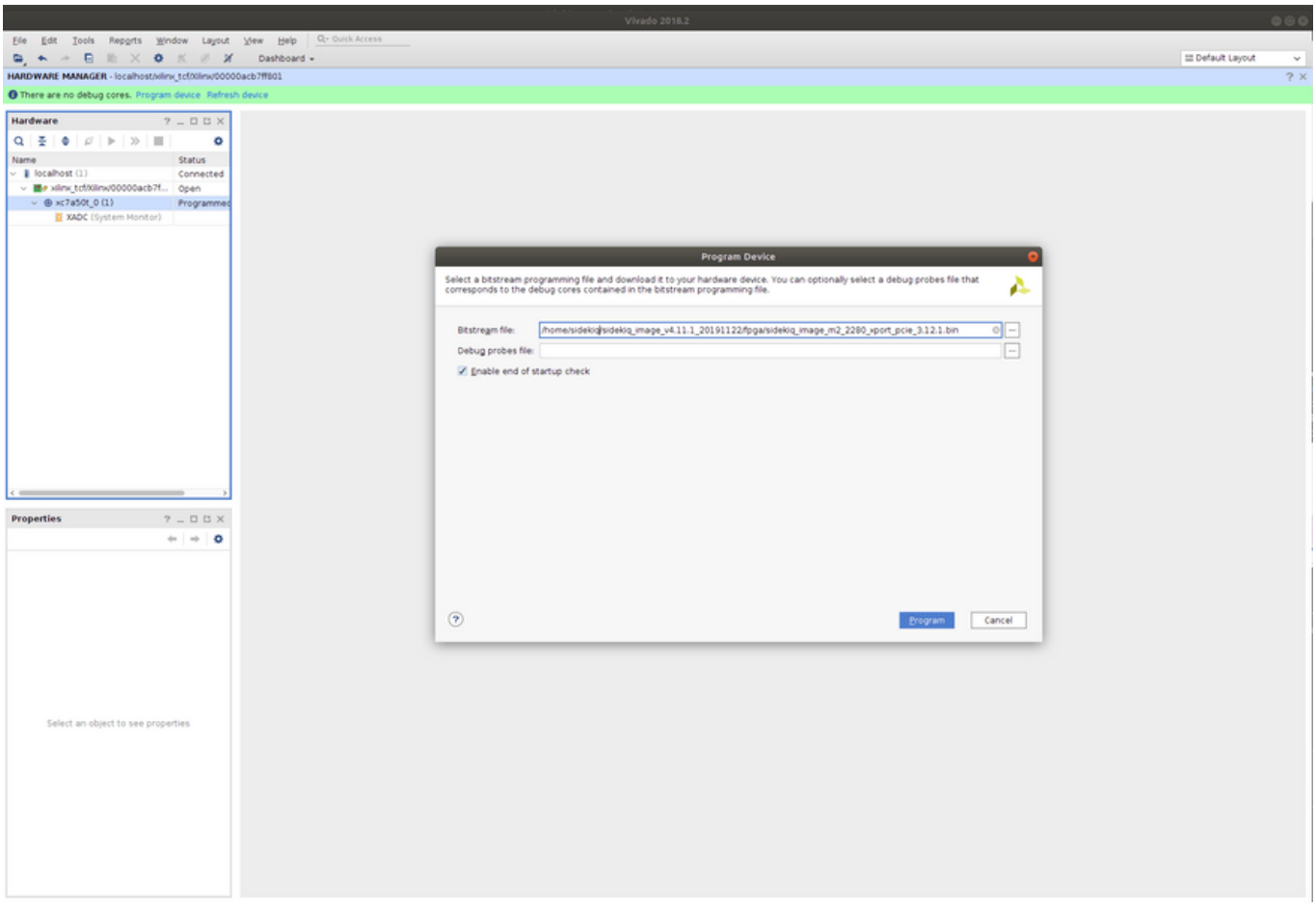

Figure 10: *Sidekiq NV100 Vivado*

Rescan the PCI bus to enumerate Sidekiq NV100

```
$ echo 1 | sudo tee /sys/bus/pci/rescan
$ lspci -d 19aa:
0a:00.0 Signal processing controller: Device 19aa:2280 (rev 04)
```

6. Reload the Sidekiq drivers

```
$ sudo ~/sidekiq_image_current/driver/load_sidekiq_drivers.sh
~/sidekiq_image_current/driver/
```

7. Download the latest *sidekiq_hardware_updater* from the Epiq Solution Support forum in the Sidekiq System Updates section located here: https://support.epiqsolutions.com/viewforum.php?f=125

8. Update Sidekiq NV100 using the *sidekiq_hardware_updater*

```
$ sudo ./sidekiq_hardware_updater_for_v4.17.sh all
```

SIDEKIQ NV100 MECHANICAL OUTLINE

A dimensioned mechanical drawing of Sidekiq NV100 is shown in the dimensioned drawing below. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.

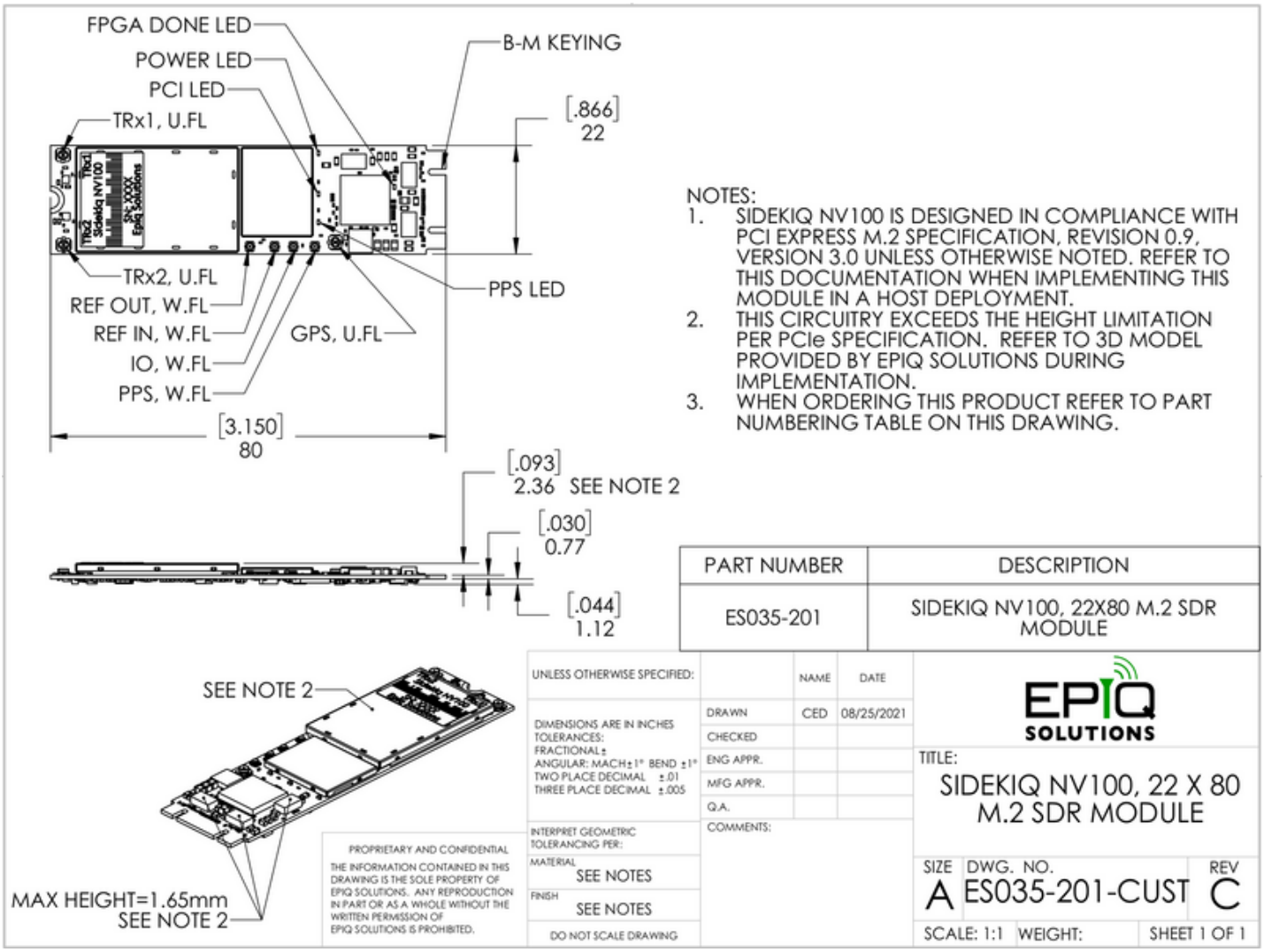

Figure 11: *Sidekiq NV100 dimensioned drawing*

SIDEKIQ NV100 RF FRONT END

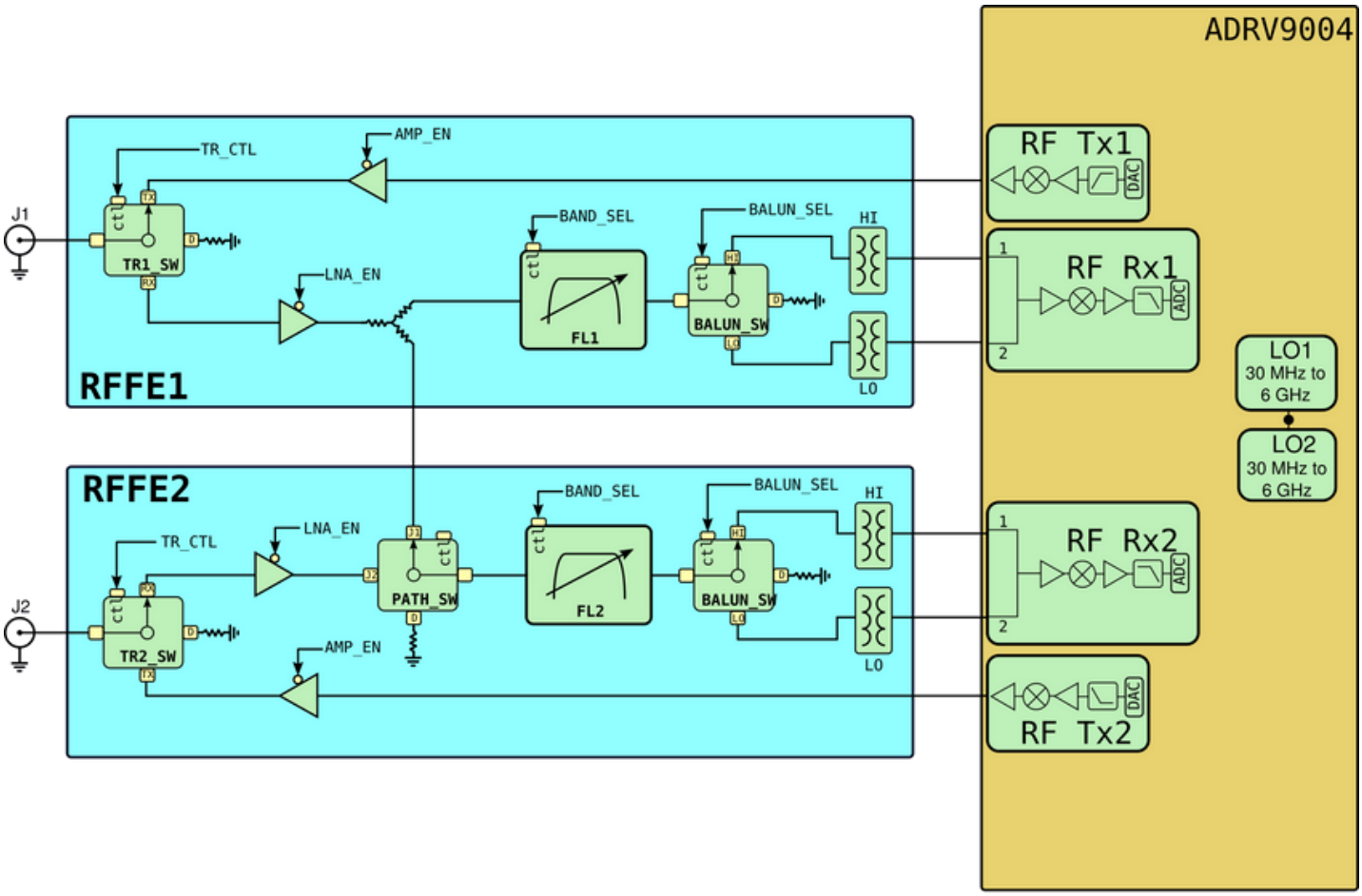

Figure 12: *Sidekiq NV100 RF Front End Block Diagram*

Note: The appropriate path through the filter banks is selected automatically based on the tune frequency.

Filter Band	LO Tune Range
low-pass filter	30 – 450 MHz
390 – 620 MHz	450 – 600 MHz
540 – 850 MHz	600 – 800 MHz
770 – 1210 MHz	800 – 1200 MHz
1130 – 1760 MHz	1200 – 1700 MHz
1680 – 2580 MHz	1700 – 2700 MHz
2500 – 3880 MHz	2700 – 3600 MHz
3800 – 6000 MHz	3600 – 6000 MHz

Table 20: *Sidekiq NV100 Rx pre-select filter bands*

STATEMENT OF VOLATILITY

Model	Sidekiq NV100
Part Number	ES035-103
Manufacturer	Epiq Solutions
Address	3740 Industrial Avenue Rolling Meadows, IL 60008

Table 21: *Model, Part Number, and Manufacturer Info*

Memory Type	Memory Size	User Modifiable	Purpose	Process to Clear
On-Chip XC7A50T FPGA BRAM	2.7 Mb	Yes	Application usage	Power-off
On-Chip XC7A50T FPGA DRAM	600 Kb	Yes	Application usage	Power-off
On-Chip ADRV9004 RFIC	unknown	Yes	RFIC ARM memory and configuration space	Power-off

Table 22: *Sidekiq NV100 Volatile Memory*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
NOR Flash	128 Mb	Yes	No	Holds FPGA bitstream(s)	Cleared with Linux utilities
EEPROM	128 Kb	No	No	Contains part number, revision, and serial number information	Must be returned to factory to clear

Table 23: *Sidekiq NV100 Non-Volatile Memory*

PREDICTED FAILURE RATE AND MTBF

Listed below is the Failure Rate and MTBF for the ES035-201-B1 Sidekiq NV100 Assembly. The calculations are derived from Relyence Reliability Software and based off a fixed/ground/controlled operating environment with an ambient temperature of 25°C.

Part Number	ES035-201-B1
Description	Sidekiq NV100 Assembly
Failure Rate (fpmh)	3.514515
MTBF (hours)	284,534.32
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 24: *Sidekiq NV100 Failure Rate and MTBF*