Sidekiq™ Mini PCIe

RF Transceiver • Low SWaP

HARDWARE USER MANUAL

V1.4 - DECEMBER 03, 2021

CHANGELOG

Revision	Date	Description	Author
0.1	2014-04-02	Initial version	Barry L
0.2	2014-05-02	Updates with substantially more technical details	Barry L
0.4	2014-05-09	Added JTAG section	Barry L
0.5	2014-05-17	-Corrected reference to SMBus interface on MiniPCIe edge connector (lines aren't hooked up by default) -Swapped Xilinx/Digilent JTAG header pins on JTAG board diagram	Barry L
0.6	2014-07-04	Added Sidekiq dimensioned drawing	Barry L
0.7	2014-08-11	Updated Sidekiq MiniPCIe pinout to specify preferred GPIO signals between host and Sidekiq, as well as preferred PPS signal between host and Sidekiq	Barry L
0.8	2015-09-03	-Added specs for external ref clock input -Updated example power consumption numbers to match RevC hardware -Added electrical specification table	Barry L
0.9	2017-11-02	-Updated section 8.3 to include component temperature ratings -Added section 10.4 discussing thermal dissipation recommendations -Updated Table 3 (MiniPCIe pinout) to include FPGA I/O pins reserved for use by Dropkiq HF/VHF low frequency extension card -Added section 10.6 to clarify use of internal vs external reference clocks -Added section 10.7 discussing the maximum RF input power levels -Updated power consumption info	Barry L
1.0	2018-05-28	-Updated figure 2 by adding accelerometer axis orientation & temperature sensor location -Added section 9.8 accel & temp sensor device part numbers -Added nominal tolerance of the 3.3V rail to section 10.3 -Updated section 9.5 External 1PPS Input, 2.5V logic-level -Added libsidekiq handles / RF port mapping information tosections 9.1, 9.2, and created table 2 -Updated section 9.6, table 3 input level 0dBm -Updated section 8.2 Gain Control Range -Added description to table 4, pin#52 -Added doc hyper-links & updated URLs. -Updated Windows OS info in sections 10.1.2 & 10.5 -Added Appendix A	Barry L
1.1	2019-08-27	Updated table 3, added Appendix B	Barry L
1.2	2020-02-25	Added section 12, updated Appendix A	Barry L
1.3	2020-09-03	Markdown conversion, updated JTAG section	Barry L
1.4	2021-12-03	Added NUC 8 and NUC 11 GPIO tables, format cleanup	Barry L

DISCLAIMER

Epiq Solutions is disclosing this document (“Documentation”) as a general guideline for development. Epiq Solutions expressly disclaims any liability arising out of your use of the Documentation. Epiq Solutions reserves the right, at its sole discretion, to change the Documentation without notice at any time. Epiq Solutions assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Epiq Solutions expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. THE DOCUMENTATION IS DISCLOSED TO YOU “AS IS” WITH NO WARRANTY OF ANY KIND. EPIQ SOLUTIONS MAKES NO OTHER WARRANTIES, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. IN NO EVENT WILL EPIQ SOLUTIONS BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

TABLE OF CONTENTS

INTRODUCTION

This document provides an overview of Epiq Solutions' Sidekiq SDR [1], a MiniPCIe card with integrated RF tuner, FPGA, and PCIe/USB interfaces to a host. The following topics will be discussed:

- Overview of the Sidekiq hardware and available interfaces
- Sidekiq usage/integration options
- Sidekiq JTAG breakout board usage
- Sidekiq NUC Platform Development Kit (PDK)

All documentation and support for Sidekiq is provided through Epiq Solutions' support website [2], which can be found at:

https://support.epiqsolutions.com

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. The user of the Sidekiq and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

The Sidekiq unit is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq unit can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation
    - A max input of -10 dBm is recommended
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

OVERVIEW

This guide provides an overview of the Sidekiq software defined radio hardware platform, associated capabilities, and basic usage. This includes the following:

- System level block diagram of the platform
- Overview of the externally accessible hardware ports
- Powering the system up and down

All documentation and support for Sidekiq is provided through Epiq Solutions' support website [2] which can be found at: https://support.epiqsolutions.com

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

REFERENCES

1. **Sidekiq Product Page**

   https://epiqsolutions.com/rf-transceiver/sidekiq
2. **Epiq Solutions Support Page**

   https://suppport.epiqsolutions.com
3. **Lenovo Group, Ltd**

   https://lenovo.com
4. **Dell, Inc**

   https://dell.com
5. **Expresscard Wikipedia Page**

   https://en.wikipedia.org/wiki/ExpressCard
6. **Expresscard-to-MiniPCIe Adapter Product Page**

   https://www.mfactors.com/products/PE3B-252d-Mini-PCIe-Card-to-ExpressCard-adapter.html
7. **Sidekiq FPGA Developer's Manual**

   https://epiqsolutions.com/downloads/sidekiq-mini-pcie/
8. **Berquist Thermal Gap Pad Material**

   https://www.henkel-adhesives.com/us/en/products/thermal-management-materials.html

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
COTS	Commercial Off The Shelf
D/A	Digital to Analog converter
dB	Decibel
dBm	Decibels referenced to one milliwatt (mW)
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
GHz	gigaherz
GPIO	General Purpose Input / Output (I/O)
GPS	Global Positioning System
HSC	Murata brand of micro-miniature RF coax connector, manufactured for use as the antenna interface on M.2 cards
IF	Intermediate Frequency
I/Q	In-Phase / Quadrature Phase
JTAG	Joint Test Action Group
kHz	kilohertz
LED	Light Emitting Diode
MHF4	Micro miniature RF coax connector, manufactured for use as the antenna interface on M.2 cards
MHz	megahertz
MIMO	Multiple Input Multiple Output
ms	millisecond
PDK	Platform Development Kit
PPS	Pulse Per Second
PPM	Parts Per Million
RF	Radio Frequency
Rx	Receive
SDK	Software Development Kit
SDR	Software Defined Radio
TCVCXO	Temperature Compensated Voltage Controlled Crystal Oscillator

TDD	Time-division duplex
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
W.FL	Micro-Miniature RF coaxial connector manufactured by Hirose

Table 1: *Terms and Definitions*

SYSTEM OVERVIEW

Sidekiq is a miniature software defined radio card in a MiniPCIe form factor, providing a flexible wideband RF transceiver that can be used by a host system. The features of the platform include the following:

- RF transceiver covering 70 MHz to 6 GHz, with independent Tx and Rx frequencies
- Supports RF channel bandwidths up to 50 MHz
- A/D and D/A quadrature sample rates from 200 Ksamples/sec up to 61.44 Msamples/sec, with 12-bit precision
- User programmable FPGA for signal processing applications (Xilinx Spartan 6 LX45-T, part # XC6SLX45T-3CSG324I)
- SPI flash for storage and automatic FPGA bitstream loading at boot-up (Micron N25Q032A11)
- On-board 40 MHz TCVCXO, with support for external reference clock input
- 8051-compatible microcontroller providing a USB 2.0 high speed interface to the host platform (Cypress FX2-based CY7C68053)
- PCIe x1 interface to the host platform
- Support for external 1PPS input signal for sample time alignment across multiple Sidekiq units
- Dimensions: 30mm x 51mm x 5mm
- Weight: 8 grams
- Power: ~2 W (application dependent)

Two different versions of Sidekiq are available:

- **SKIQ-001** supports operation as a two-channel phase coherent RF receiver, or as a 1x1 RF transceiver (with one RF receiver and one RF transmitter)
- **SKIQ-002** supports operation as a 1x1 RF transceiver (with one RF transmitter and one RF receiver)

For the purposes of this document, the remaining documentation will be in reference to SKIQ-001. A block diagram of Sidekiq is shown in the figure below.

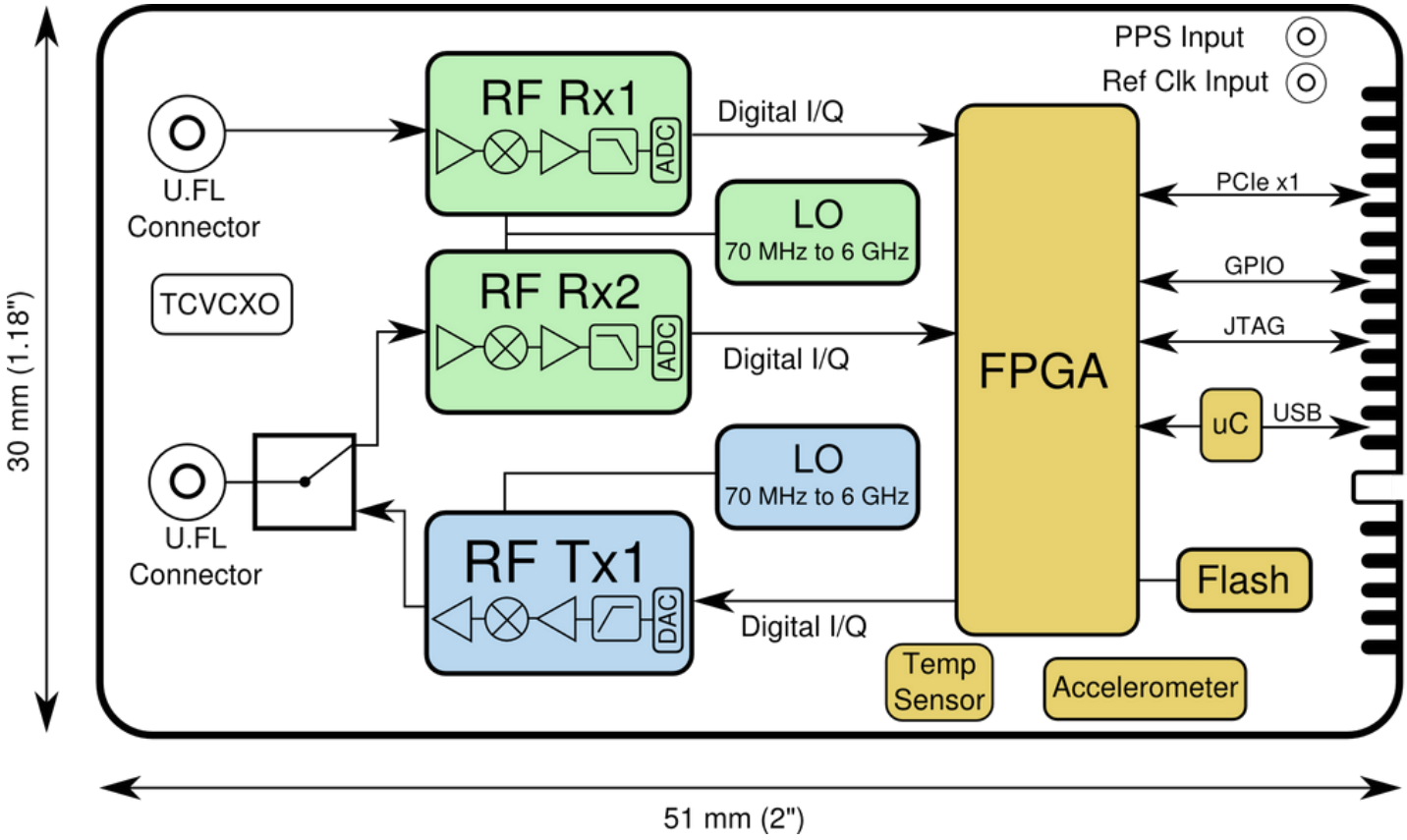

Figure 1: *Block diagram of the Sidekiq MiniPCIe card*

HARDWARE SPECIFICATION

RF RECEIVER SPECIFICATION

RF Input	U.FL miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	70 MHz to 6 GHz
Tuning Step Size	~2.4 Hz
Tuning Time	~1 mS
Typical Noise Figure	8 dB
Typical IIP3	-10 dBm
Max RF Input Power Level	See Maximum RF Power Input in RF Input Connector section
Gain Control Range	0 to 76 dB, 1 dB steps
A/D Converter Sample Rate	200 Ksamples/sec to 61.44 Msamples/sec
A/D Converter Sample Width	12 bits
Typical I/Q balance	> 60 dB
On-board Reference Clock	40 MHz, +/- 1PPM accuracy (shared with Tx)

Table 2: *RF Receiver Specs*

RF TRANSMITTER SPECIFICATION

RF Input	U.FL miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	70 MHz to 6 GHz
Tuning Step Size	~2.4 Hz
Tuning Time	~1 mS
Gain Control Range	0 to 89.75 dB, 0.25 dB steps
RF Output Power	+13 dBm < 2 GHz, +10 dBm above 2 GHz
D/A Converter Sample Rate	200 Ksamples/sec to 61.44 Msamples/sec
D/A Converter Sample Width	12 bits

Typical I/Q balance	> 60 dB
On-board Reference Clock	40 MHz, +/- 1PPM accuracy (shared with Rx)

Table 3: *RF Transmitter Specs*

HARDWARE SPECIFICATION

FPGA	Xilinx Spartan-6 LX45T (speed grade “-3I”) with x1 PCIe interface to host
USB	Cypress FX2 microcontroller with USB 2.0 high-speed interface to host
FPGA Reprogramming	Over USB or PCIe
Accelerometer	3-axis
Temperature Sensor	-55 deg C to +125 deg C (+/- 2 deg C resolution)
Component Temperature Rating	-30 deg C* to + 85 deg C *Operation down to -40 deg C is supported, though the TCVCXO will operate outside of the +/- 1PPM accuracy specification.

Table 4: *Hardware Specs*

HARDWARE INTERFACES

Sidekiq provides a variety of different hardware interfaces for use by an end user. Each of these hardware interfaces is shown below.

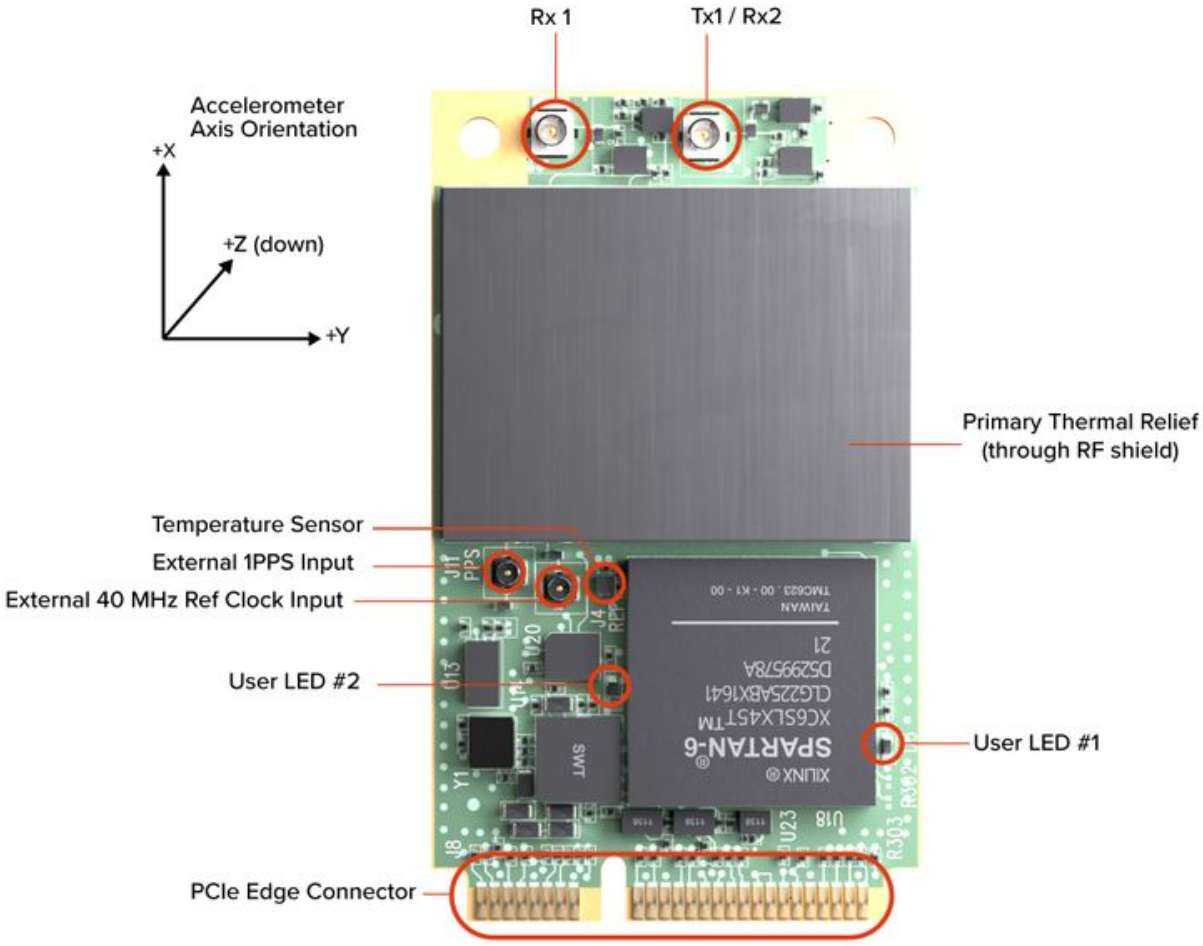

Figure 2: *Annotated diagram of Sidekiq hardware I/O interfaces*

RX1

The Rx1 interface is a U.FL jack connector that provides an RF input path for the primary RF receiver in Sidekiq. U.FL is the standard interface utilized by MiniPCIe cards, and thus many host systems supporting MiniPCIe are already pre-wired with antennas that terminate with a U.FL plug connector. This Rx port supports RF input frequencies between 70 MHz and 6 GHz. The libsidekiq software library RxA1 handle (sidekiq_rx_hdl_A1) is mapped to the Rx1 interface.

TX1 / RX2

The Tx1 / Rx2 interface is a U.FL jack connector that provides access to either the primary RF transmitter or the secondary RF receiver in Sidekiq. U.FL is the standard interface utilized by MiniPCIe cards, and thus many host systems supporting MiniPCIe are already pre-wired with antennas that terminate with a U.FL plug connector. This port supports RF frequencies between 70 MHz and 6 GHz. The libsidekiq software API provides the facility for selecting whether this port is configured for reception or transmission, and sets an on-board RF switch appropriately.

This port can provide access to both Tx1 (sidekiq_tx_hdl_A1) and Rx2 (sidekiq_rx_hdl_A2), where the operating mode can be selected through software. The ability to switch between Tx and Rx on this antenna port is controlled from the FPGA, and is accessible via the libsidekiq software library.

Handle	RF Port
skiq_rx_hdl_A1	skiq_rf_port_Jxxx_RX1
skiq_rx_hdl_A2	skiq_rf_port_Jxxx_TX1RX2
skiq_tx_hdl_A1	skiq_rf_port__Jxxx_TX1RX2

Table 5: *RF Port Mapping introduced in libsidekiq v4.6.0*

USER LED #1

The User LED #1 provides a visual status indicator that can be controlled through the libsidekiq software API. By default, this LED is used to provide an indication that a PCIe link has been successfully negotiated between the host CPU and the FPGA on Sidekiq. When this LED is illuminated, a link has been established. When the LED is not illuminated, a link is not established. During FPGA reprogramming, PCIe link is lost and then re-established after the bitstream has been successfully loaded.

USER LED #2

The User LED #2 provides a visual status indicator that can be controlled through the libsidekiq API. By default, this LED is used to provide an indication that the FPGA has successfully loaded and is running an FPGA bitstream.

EXTERNAL 1PPS INPUT

The External 1PPS Input interface is a W.FL jack connector that allows an external 1PPS signal to be brought in to the on-board FPGA (2.5V logic-level) on Sidekiq for use in time synchronization. A

maximum of 3.3V can be safely applied to this input port. This 1PPS input is optional. Note: Since this signal is routed directly into the on-board FPGA, it is possible to also use this signal as a general purpose input. Contact Epiq Solutions for details of alternate usage of this port.

EXTERNAL REFERENCE CLOCK INPUT

The External Reference Clock Input interface is a W.FL jack connector that allows an external 40 MHz reference clock to be brought in to Sidekiq and utilized instead of the default on-board 40 MHz TCVCXO. This provides the facility to have multiple Sidekiq cards share a common external 40 MHz reference clock. Note: On RevB Sidekiq cards, a hardware modification (resistor swap) is required to disable the on-board 40 MHz TCVCXO, and to accept the external 40 MHz reference clock input. Contact Epiq Solutions for details. RevC Sidekiq and beyond provide a means to switch between the on-board reference clock and external reference clock through the libsidekiq software API.

The electrical specification for this input signal is defined below.

Input Level	0.8 – 1.3 Vpp, 0 dBm max from 50 ohm source
Input Impedance	AC-Coupled high impedance
Frequency	40 MHz
Waveform	Square or Sinewave
Connector Type	W.FL

Table 6: *Electrical specification for external reference clock input*

PRIMARY THERMAL RELIEF (RF SHIELD)

The RF shield (used to minimize the effects of RF noise entering the RF front end) serves as the primary thermal relief path for heat dissipation in the system. Underneath the shield, thermal gap pad material is used to transfer heat from components to the shield itself, yielding a minimal thermal resistance. If no air flow is available in the host system where Sidekiq is being integrated, it is highly recommended that the user provide a thermal dissipation path from this shield to a thermally conductive surface in the host system, such as a metal back plate or other metal housing. The use of thermal gap pad material [8] can provide a flexible yet efficient thermal path between the RF shield and the host system.

In addition to the RF shield, the other primary component generating heat in Sidekiq is the Xilinx Spartan 6 FPGA (which is located right next to the RF shield). If an end user is developing a thermal dissipation path for the RF shield, it is also recommended to include the FPGA in the thermal

transfer path as well. Similar to the RF shield, use of a thermal gap pad material can be very effective in ensuring good thermal conductivity between this component and the host system.

SIDEKIQ ACCELEROMETER & TEMPERATURE SENSOR

The Sidekiq is equipped with temperature and accelerometer devices.

- Analog Devices 3-Axis Accelerometer ADXL346ACCZ
- Texas Instruments Temperature Sensor TMP103AYFFR

Please refer to the annotated diagram for the Sidekiq accelerometer axis orientation & temperature sensor location.

The libsidekiq software API provides access to these peripherals, test applications *read_accel* and *read_temp* are included with the sidekiq software.

Additional information can be found in the Sidekiq Software Development manual.

MINIPCIE EDGE CONNECTOR

The MiniPCIe Edge Connector is used to route various signals between the MiniPCIe host system and the Sidekiq card. A complete table enumerating the pins and their usage on Sidekiq is shown in the following table.

Pin #	MiniPCIe Pin Name	Description as used in Sidekiq		Pin #	MiniPCIe Pin Name	Description as used in Sidekiq
1	WAKE_	Wakeup signal routed to both FX2 as well as FPGA (pin N18, 2.5V I/O)		27	GND	Ground
2	+3.3Vaux	+3.3V supply		28	1.5V	Unused (floating)
3	COEX1	-GPIO routed to FPGA pin J7, 2.5V I/O -Used as RESET_ signal for Dropkiq HF/VHF low frequency extension card		29	GND	Ground
4	GND	Ground		30	SMB_CLK	Not connected by default (to prevent I2C address conflicts with host)
5	COEX2	GPIO routed to FPGA pin J6, 2.5V I/O		31	PETn0	PCIe differential transmit lane 0, negative leg

6	1.5V	Unused (floating)		32	SMB_DATA	Not connected by default (to prevent I2C address conflicts with host)
7	CLKREQ_	PCIe clock request		33	PETp0	PCIe differential transmit lane 0, positive leg
8	UIM_PWR	Unused (floating)		34	GND	Ground
9	GND	Ground		35	GND	Ground
10	UIM_DATA	JTAG TDI (when connected to the Sidekiq JTAG pod)		36	USB_D-	USB 2.0 high speed data, negative leg
11	REFCLK-	PCIe reference clock, negative leg		37	GND	Ground
12	UIM_CLK	JTAG TDO (when connected to the Sidekiq JTAG pod)		38	USB_D+	USB 2.0 high speed data, positive leg
13	REFCLK+	PCIe reference clock, positive leg		39	+3.3Vaux	+3.3V supply
14	UIM_RESET	JTAG TMS (when connected to the Sidekiq JTAG pod)		40	GND	Ground
15	GND	Ground		41	+3.3Vaux	+3.3V supply
16	UIM_SPU	JTAG TCK (when connected to the Sidekiq JTAG pod)		42	LED_WWAN_	-GPIO routed to FPGA pin A3, 2.5V I/O -Used as I2C SDA signal to control Dropkiq HF/VHF low frequency extension card if installed
17	UIM_IC_DM	GPIO routed to FPGA pin D15, 2.5V I/O		43	GND	Ground
18	GND	Ground		44	LED*WLAN*\	-GPIO routed to FPGA pin B3, 2.5V I/O-Used as SPI enable signal to control Dropkiq HF/VHF frequency extension card if installed
19	UIM_IC_DP	GPIO routed to FPGA pin E14, 2.5V I/O		45	RESERVED4*	-GPIO routed to FPGA pin F2, 2.5V I/O-Used as SPI clock signal to control Dropkiq HF/VHF frequency extension card if installed
20	W_DISABLE1_	GPIO routed to FPGA pin E12, 2.5V I/O		46	LED_WPAN_	-GPIO routed to FPGA pin A2, 2.5V I/O-Used as I2C SCL signal to control Dropkiq HF/VHF frequency extension card if installed
21	GND	Ground		47	RESERVED3*	-GPIO routed to FPGA pin F1, 2.5V I/O-Used as SPI MOSI signal to control Dropkiq HF/VHF frequency extension card if installed
22	PERST_	PCIe reset		48	1.5V	Unused (floating)
23	PERn0	PCIe differential receive lane0, negative leg		49	RESERVED2*	-GPIO routed to FPGA pin H3, 2.5V I/O-Used as SPI MISO signal to control Dropkiq HF/VHF frequency extension card if installed
24	+3.3Vaux	+3.3V supply		50	GND	Ground

25	PERp0	PCIe differential receive lane0, positive		51	W_DISABLE2_	Routed to SYNC_IN pin of AD936x RFIC
26	GND	Ground		52	+3.3Vaux	+3.3V supply

Table 7: *Sidekiq MiniPCIe edge connector signal descriptions*

* This indicates a GPIO pin that should preferred for use when interfacing to a custom host platform. These pins will receive priority in terms of GPIO backward compatibility if future variants of Sidekiq require changes to the GPIO allocation.

BASIC USAGE IN A HOST SYSTEM

HOST SYSTEM COMPATIBILITY

From a hardware perspective, Sidekiq is compatible with any host system that provides a standards-compliant MiniPCIe card slot. However, there are several points to note regarding the usage of Sidekiq in different host system. The following section provides an overview of these details.

BIOS COMPATIBILITY

Different host systems enforce different rules regarding which MiniPCIe cards are considered to be compatible with their platform In some cases, such as laptops manufactured by Lenovo [3], the BIOS of the computer will probe the MiniPCIe slots to identify the type/manufacturer of the card installed at power-up. If the detected card is not in a pre-defined “white list” of compatible cards, the host system will not continue booting up. Other laptops, such as those manufactured by Dell, Inc. [4], have no such restrictions. It is recommended that the end user verify whether or not their intended host system imposes any limitations regarding compatible cards.

Note: this only applies to internal MiniPCIe cards. Using Sidekiq in an external MiniPCIe-to-Expresscard adapter, or an internal MiniPCIe-to-PCIe adapter does not present any issues.

OPERATING SYSTEM COMPATIBILITY

Windows 7 and 10 are currently supported. Windows 7 support was added in the Sidekiq SDK v4.4.0 release and Windows 10 support was added in the Sidekiq SDK v4.6.0 release.

Various Linux kernel versions have been tested starting at version 3.0. Sidekiq has been tested both in x86-based Linux systems as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported. Please contact Epiq Solutions for details.

For customers interested in doing a custom build of the Sidekiq PCIe device driver for their host platform, a license for the source code for this device driver is also available separately. Please contact Epiq Solutions for details.

SIGNALING INTERFACES

Sidekiq is intended to operate in host systems that provide a full-featured MiniPCIe interface, including both PCIe as well as USB signalling. The PCIe interface serves as the primary bridge to perform both control operations between the host system and Sidekiq, as well as data streaming operations between the host system and Sidekiq. The USB interface provides a mechanism to update the FPGA bitstream at run-time from the host system. This FPGA re-programming operation

temporarily brings down the PCIe interface, and thus the PCIe interface can't be used during this time.

Note: Future updates to the libsidekiq software library and FPGA reference design will allow the USB interface to be used as the primary bridge to perform both control operations and data streaming operations between the host system and Sidekiq (though streaming operations will be reduced due to the limited bandwidth of the USB 2.0 bus compared to PCIe). Similarly, support for reprogramming the SPI flash holding the default FPGA design is also planned, thus allowing host systems to reprogram the FPGA bitstream without the USB interface wired up in the MiniPCIe slot.

RF INTERFACES

Many host systems that support MiniPCIe come pre-wired with antennas already integrated in to the host system. These antennas typically terminate in U.FL connectors, since this is the standard that is defined for use by MiniPCIe cards. The range of RF frequencies supported by the antennas, as well as the gain of the antennas, will be platform specific. Typically, these internal antennas have support for cellular frequencies (700 MHz to 1 GHz, and 1700 MHz to 2.1 GHz), as well as WiFi frequencies (2.4 GHz and 5.9 GHz), but it is up to the user to validate the performance of the antenna solution. Sidekiq has two U.FL antenna ports which are compatible with antennas in the host system.

SYSTEM INTERFACE OPTIONS

Sidekiq can be interfaced to a host system through different electrical/physical interfaces. The following sections provide details of several potential options.

Note: Sidekiq should never be inserted into or removed from a host system with power applied to the host system. This could permanently damage the card. *The one exception to this is when using Sidekiq with an Expresscard adapter. See Expresscard slot section for details.*

MINIPCIE SLOT

The most common method for interfacing Sidekiq to a host system, such as a laptop or an embedded single board computer, is through a built-in MiniPCIe slot in the host system. This provides the most compact interfacing option from a size perspective, though may require some level of dis-assembly of the host system to access the card slot. Typical MiniPCIe slots provide both a x1 PCIe interface as well as a USB 2.0 high speed interface. Consult the host system documentation to confirm the available signaling options.

EXPRESSCARD SLOT

Many laptops provide an external Expresscard [5] slot to allow a user to interface peripherals to their host system. Standards-compliant Expresscard slots provide both a x1 PCIe interface as well as a

USB 2.0 high speed interface to the host. Sidekiq can be used with an Expresscard-to-MiniPCIe adapter, though Sidekiq does not currently support the typical hot-swap facility provided by Expresscard slots. The Sidekiq PDK laptop ships with an Expresscard-to-MiniPCIe adapter [6] to support evaluation.

In addition, Epiq Solutions is developing a version of the Expresscard-to-MiniPCIe adapter with a housing around the Sidekiq card, terminating with two SMA ports on the end of the housing. Please contact Epiq Solutions for details of this adapter plus housing.

PCIE SLOT

The majority of the computer motherboards manufactured today come with at least one PCIe expansion slot. These slots are typically used to add peripherals to the host computer, such as network cards etc. Several manufacturers make PCIe-to-MiniPCIe adapter cards that can be used to allow Sidekiq to interface to a host system's PCIe slot. These slots only provide the PCIe interface natively, so the USB interface is often broken out to a separate USB connector on the PCIe-to-MiniPCIe adapter card. This allows the user to plug a USB cable in between the adapter card and another available USB port in the host system.

POWER CONSUMPTION

The power consumption of Sidekiq varies depending on the configuration and application of the card. Host systems supporting MiniPCIe typically provide a maximum of ~3W of power on the 3.3V rail to each MiniPCIe card, so this sets the upper bounds of what Sidekiq can consume. Nominal tolerance of the 3.3V rail is +/-9%. The following table provides a listing of power consumption under different operating conditions. Note that each of these assumes that the stock Sidekiq FPGA reference design loaded in to the FPGA.

Test Scenario	Power Consumption (in Watts)
Test scenario #1:-Card powered up but idle (no Tx or Rx)	1.12 W
Test scenario #2:-Card powered up, single channel Rx tuned to 850 MHz streaming over PCIe at a sample rate of 30 Msamples/sec	2.0 W
Test scenario #3:-Card powered up, single channel Rx tuned to 850 MHz streaming over PCIe at a sample rate of 30 Msamples/sec, single channel Tx tuned to 3.8 GHz (Tx attenuation=0) streaming over PCIe at a sample rate of 30 Msamples/sec	2.43 W

Table 8: *Example power consumption estimates for Sidekiq RevC*

THERMAL DISSIPATION

Effective use of Sidekiq in a system also requires consideration of an appropriate thermal dissipation solution. Since Sidekiq can be integrated into a variety of different host systems with different thermal profiles (i.e., forced air, natural convection, etc), the end user is required to perform their own system analysis to determine what level of thermal dissipation is appropriate for their use-case. Sidekiq uses components that are rated for operation to +85 deg C, and thus the end user must ensure that the temperature reported by the on-board temperature sensor does not exceed +85 deg C.

Exceeding the maximum rated temperature of +85 deg C may damage the Sidekiq card and/or accelerate failure of the card.

As discussed in the Primary Thermal Relief (RF Shield) section, both the RF shield as well as the FPGA are the two primary sources of heat requiring thermal dissipation. It is highly recommended that a thermal transfer solution, such as gap pad [8], be used to provide a thermal dissipation path between the RF shield/FPGA and an external conduction surface in the host system. With adequate thermal transfer to the host system, it is common for Sidekiq to report steady state board temperatures in the range of 50 deg C to 55 deg C while fully operational, with an ambient temperature of 25 deg C. Note: The actual temperature range achievable in a given system may vary substantially depending on a number of factors, including the number of RF receivers operational, the A/D and D/A sample rates, customizations done to the FPGA, and others. Again, it is strongly recommended that a thorough system evaluation be performed by the customer to fully characterize the thermal profile of Sidekiq in their system. Please refer to the annotated diagram for the temperature sensor location.

PROPER DETECTION OF SIDEKIQ IN A HOST SYSTEM

A properly configured Windows host system (with the necessary device driver loaded) with both PCIe and USB 2.0 will allow the Sidekiq to enumerate on both the PCIe bus as well as the USB bus.

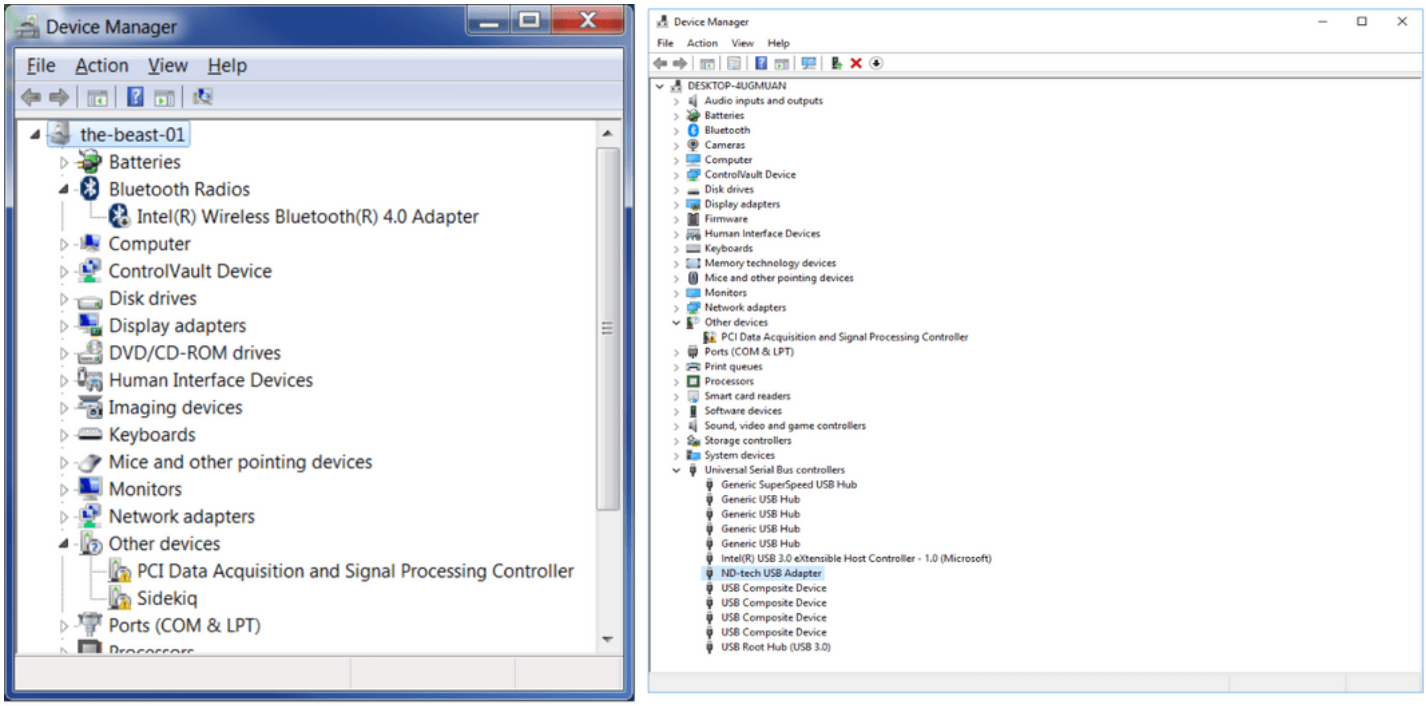

Figure 3: *Detection of Sidekiq in Windows 7 and Windows 10*

Please refer to Appendix 10 – Windows Sidekiq Development of the Sidekiq Development Manual for additional information.

A properly configured Linux host system (with the necessary dmadriver.ko device driver loaded) will allow Sidekiq to enumerate on both the PCIe bus, as well as the USB bus. The enumeration on the PCIe bus can be verified by executing the command *"lspci"* to confirm the presence of Sidekiq. The execution of *"lspci"* will provide output similar to the following when Sidekiq is detected (the detection of Sidekiq is in bold, and shows up as a "Signal processing controller":

```
00:1f.2 RAID bus controller: Intel Corporation 82801 Mobile SATA Controller [RAID mode] (rev
04)
00:1f.3 SMBus: Intel Corporation 7 Series C210 Series Chipset Family SMBus Controller (rev 04)
01:00.0 Signal processing controller: Device 19aa:e004 (rev 06)
02:00.0 Network controller: Intel Corporation Centrino Advanced-N 6205 [Taylor Peak] (rev 34)
```

Similarly, Sidekiq enumerates on the USB bus. This enumeration can be verified by executing the command *"lsusb"* to confirm the presence of Sidekiq. The execution of *"sudo lsusb -v"* will provide a verbose listing of all USB devices currently enumerated in the system, with output similar to the following when Sidekiq is detected:

```
...

Bus 001 Device 003: ID 04b4:1004 Cypress Semiconductor Corp.
Device Descriptor:
bLength18
bDescriptorType1
bcdUSB2.00
bDeviceClass0 (Defined at Interface level)
bDeviceSubClass0
bDeviceProtocol0
bMaxPacketSize064
idVendor0x04b4 Cypress Semiconductor Corp.
idProduct0x1004
bcdDevice0.00
iManufacturer1 Epiq Solutions
iProduct2 Sidekiq

...
```

INTERNAL/EXTERNAL REFERENCE CLOCK OPTIONS

Sidekiq supports options to use either an internal (i.e. on-board) 40 MHz TCVCXO as a reference clock, or an external 40 MHz reference clock as defined in the External Reference Clock Input section. Regardless of which clock source is selected, this clock serves as the reference for both the RF front end as well as the digital processing blocks in the FPGA. The selection of whether Sidekiq uses the internal reference clock or the external reference clock is stored as a configuration parameter in EEPROM on the card[1]. This parameter is read by a microcontroller on-board Sidekiq at power-up, and is used to configure how the card should operate.

If Sidekiq is configured to use an external reference clock, but no external reference clock is provided via the W.FL connector, any application attempting to initialize the Sidekiq card will fail.

For cases where a customer would like to switch between internal and external reference clock options, a software application can be provided to update the EEPROM configuration settings. Please contact Epiq Solutions for details.

MAXIMUM RF POWER INPUT AT RF INPUT CONNECTOR

It is often necessary for the system integrator to understand the maximum RF input signal that can be received by Sidekiq. The maximum acceptable RF power input at the Rx U.FL connector depends on the operating mode of the card:

- If the RF receiver is tuned <= 3 GHz (which uses the “low band” Rx path), and RF input signals are being received below 3 GHz, the maximum allowable RF input power level at the U.FL Rx connector without causing damage is +23 dBm. Note: An RF overload protection circuit automatically engages when the RF input power level reaches approximately -15 dBm to protect the hardware up until the +23 dBm input level.

- If the RF receiver is tuned > 3 GHz (which uses the “high band” Rx path), and RF input signals are being received > 2 GHz, the maximum allowable RF input power level at the U.FL Rx connector without causing damage is -8 dBm. Note: The “high band” Rx path does not have any RF overload protection circuitry in-line due to space constraints. Further, there is an LNA to increase the Rx sensitivity up to 6 GHz.
- If the RF receiver is tuned > 3 GHz (which uses the “high band” Rx path), and RF input signals are being received <= 2 GHz, the maximum allowable RF input power level at the U.FL Rx connector without causing damage is +12 dBm. Note: The 3 GHz high pass filter in-line with the “high band” Rx path provides the extra signal attenuation to increase the maximum allowed RF input signal under these conditions.

SUPPORT FOR HOST SYSTEM SLEEP/HIBERNATION

Some host systems that have a “sleep mode” or “hibernation” mode where power is no longer applied to the MiniPCIe slot while in this state. Sidekiq does not currently have proper support to handle these transitions, since the FPGA bitstream would be lost during this transition. Thus, if the host system enters in to a sleep/hibernation state, it should be assumed that the Sidekiq card will likely need to undergo a complete reboot in order to fully use all features of the card again. For example, if a Sidekiq card is installed in a laptop with power savings mode enabled each time the laptop lid closes, proper Sidekiq operation is not guaranteed after the laptop lid is re-opened.

JTAG ACCESS ON SIDEKIQ

The Xilinx Spartan 6 LX45-T FPGA utilized on Sidekiq provides a JTAG interface that can be accessed and utilized during the development of custom logic/processing modules targeting the FPGA. However, due to size constraints, there is no space available on Sidekiq for a standard JTAG interface. Thus, the JTAG interface signals are routed to the MiniPCIe edge connector (see Table 4 for pinout details). Due to the fact that no host system would typically route these signals to a JTAG header, Epiq Solutions developed a stand-alone JTAG adapter card to provide access to these JTAG signals. In this configuration, Sidekiq that can be used in conjunction with a MiniPCIe extender ribbon cable to connect the MiniPCIe signals to the host system through the MiniPCIe extender card. This allows standard FPGA JTAG programmers/debuggers, such as the Xilinx Platform USB Cable II, and the Digilent HS1 rev A 1x5 JTAG debug pod, to be used with Sidekiq. The figure below shows Sidekiq installed in the JTAG Board, with the associated MiniPCIe adapter card that can be installed in the host system. Note: No additional power source is required for the Sidekiq JTAG board. Power is derived from the host system, through the 3.3V interface provided by the MiniPCIe connector.

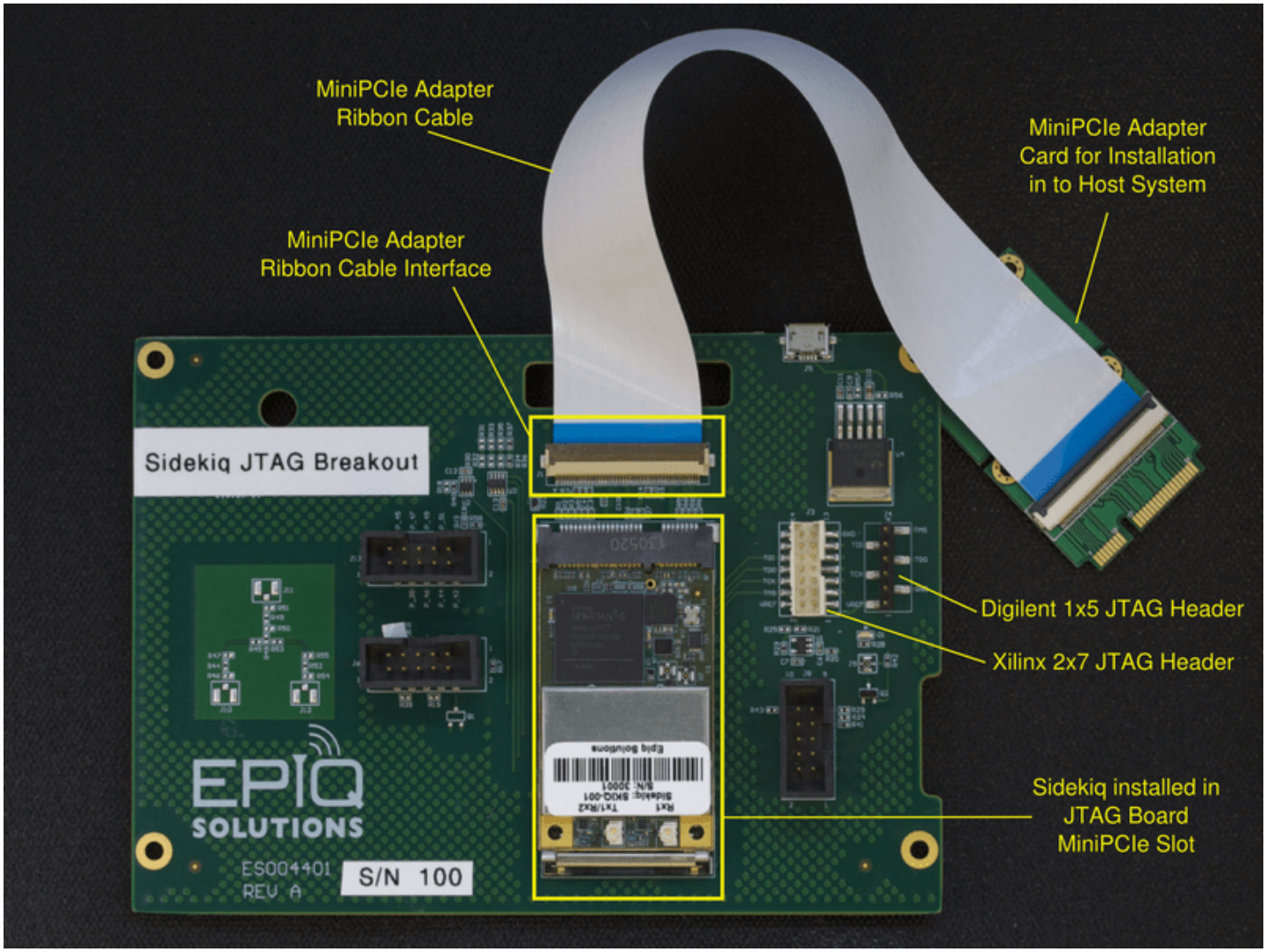

Figure 4: *Sidekiq JTAG Board plus MiniPCIe adapter card for use in debugging*

The Sidekiq JTAG board provides several additional interfaces that can be used for testing Sidekiq, such as power consumption measurement and access to the FPGA GPIO signals provided by Sidekiq at the MiniPCIe edge connector. Contact Epiq Solutions for additional details of these features.

Note: For customers designing their own mPCIe carriers, to activate the JTAG buffers on Sidekiq mPCIe: you'll need to pull mPCIe pin 6 to 3.3V (via 1Kohm resistor) and pull pin 28 low (can go directly to GND). The JTAG interface runs at 2.5V logic levels but there are buffers on Sidekiq that can handle 3.3V logic levels, if needed.

JTAG BOARD USAGE NOTES

The following section provides usage notes for the Sidekiq JTAG Board.

- Details of using Xilinx tools to program and debug FPGA bitstreams with Sidekiq can be found in the Sidekiq FPGA Developer's Manual [7]

- The Sidekiq JTAG Board is powered through the MiniPCIe interface, with power coming from the host system. No additional power supply is required for the JTAG Board.
- Only one JTAG pod should be connected to the JTAG Board at any given time. Plugging in a JTAG pod to both JTAG interfaces will damage the JTAG Board.
- The signal integrity of the MiniPCIe Adapter Card Ribbon Cable has been tested in several different systems without any issues. Longer ribbon cables may also work, though it is up to the end user to verify functionality.

SIDEKIQ MECHANICAL OUTLINE

A dimensioned mechanical drawing of Sidekiq is shown below. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.

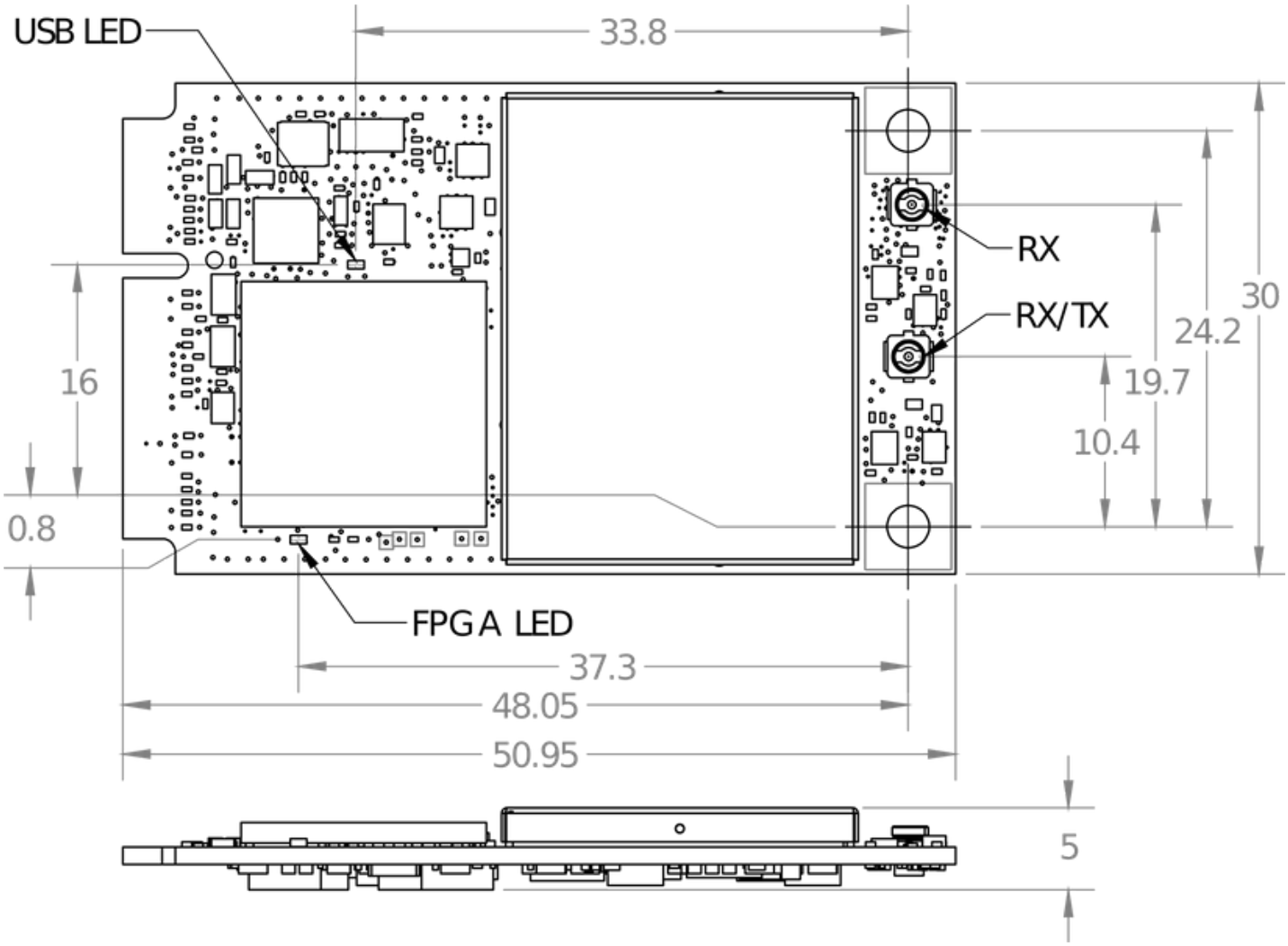

Figure 5: *Sidekiq dimensioned drawing*

SIDEKIQ NUC PLATFORM DEVELOPMENT KIT (PDK)

SIDEKIQ NUC PDK OVERVIEW

The Sidekiq NUC PDK includes one mPCIe Sidekiq hosted on an Intel NUC8I7BEH, NUC11TNHi5/i7, or later Mini PC NUC system.

The Sidekiq NUC PDK is pre-loaded with Epiq Solutions' libsidekiq API, test applications, ERA (Spectrum Analyzer), and device drivers. All support-related questions, product documentation, software, and FPGA reference designs are managed through Epiq Solutions' private web-based support forum* available at epiqsolutions.com/support.

*Registration is required to use the Epiq Solutions Customer Support Center. You can register at epiqsolutions.com/support

Figure 6: *Sidekiq NUC hardware I/O interfaces*

SIDEKIQ NUC PDK SETUP

After you have removed all of the package contents, setup the system as follows:

1. Connect a USB keyboard, mouse to available USB ports, HDMI monitor to HDMI port, a network cable to the RJ45 port, and the DC power supply cable from the provided DC power brick.
2. Connect an antenna or RF source to RX SMA before using any of the test applications or ERA; for more details, see “Sidekiq NUC RF Ports” below.
3. Power on the NUC; this will also power-on the connected TB3 chassis. The computer monitor will indicate that it is starting up Ubuntu Linux and then it will show a login page.
4. Log into Ubuntu with the user credentials:

   Username: **sidekiq** Password: **sidekiq**

INCLUDED APPLICATIONS

Several applications are included with the PDK in order to help you test and verify your setup, such as our standard Sidekiq command-line test applications and ERA, a spectrum analyzer.

Libsidekiq Test Applications are located in:

```
 /home/sidekiq/sidekiq_image_current/test_apps
```

Launch a terminal window from Dash (search for “Terminal”) or by pressing Ctrl-Alt-T.

```
cd /home/sidekiq/sidekiq_image_current/test_apps/
```

A user can scan the system for Sidekiq cards, displaying version information for one or all card(s) upon detection by running the *version_test* application by executing the command:

```
./version_test
```

The application should return results that look something like the following:

```
SKIQ[3790]: INFO Need to perform full initialization
SKIQ[3790]: INFO Performing detection of cards
SKIQ[3790]: INFO Sidekiq card detection completed
successfully!
SKIQ[3790]: INFO Preliminary initialization complete, continue
full initialization
2 card(s) found: 0 in use, 1 available!
Card IDs currently used :
Card IDs currently available: 0
Info: initializing 1 card(s)...
SKIQ[3790]: INFO libsidekiq v4.12.0
version_test[3790]: INFO Sidekiq card 0 is serial
number=#####, hardware MPCIE C (rev C), product SKIQ-MPCIE-001 (PCIe) (part ES004202-C0-00)
version_test[3790]: INFO Sidekiq card 0 firmware v2.9
version_test[3790]:INFO Sidekiq card 0 FPGA v3.13.0, (date 20011315, FIFO size 16k)
version_test[3790]: INFO Sidekiq card 0 is configured for an internal 40000000 Hz reference
clock
version_test[3790]: INFO Loading calibration data for Sidekiq PCIe, card 0

**********************************************************

* libsidekiq v4.12.0

**********************************************************
**********************************************************

* Sidekiq Card 0
Card
accelerometer present: true
part type: PCIe
part info: ES004202-C0-00
serial: 30479
xport: PCIe
FPGA version: 3.13.0
git hash: 0x06f5a1a9
build date (yymmddhh): 20011315
tx fifo size: 16k samples
FW version: 2.9
RF reference clock: internal
reference clock frequency: 40000000 Hz

**********************************************************

version_test[3790]: INFO Unlocking card 0
```

Raw I/Q Capture

A user can perform an RF capture of I/Q samples using the default configuration by executing the *rx_samples* application as follows:

```
./rx_samples -c 0 --handle=A1 -r 30.72e6 -b 25e6 -f 1e9 -d /tmp/out
```

This command will save I/Q samples to a file named */tmp/out.a1* using values for 30.72 Msps sample rate, 25 MHz channel bandwidth, 1 GHz tune frequency. The data is stored in the file as 16-bit I/Q pairs with ‘I’ samples stored in the upper 16-bits of each word, and ‘Q’ samples stored in the lower 16-bits of each word. Additional available options are described by executing:

```
./rx_samples -h
```

ERA - Epiq RF Analyzer

EPIQ RF Analyzer (ERA) is installed on the Sidekiq NUC PDK. ERA is an application that controls an Epiq radio and provides a realtime view of spectrum, radio frequency, sample rate, and filtering configuration. ERA documentation can be found on the support forum, available at support.epiqsolutions.com.

ERA Release Information

- The included version does not provide “Pro” features of ERA for (e.g. recording, see User Manual for all Pro-only features). Future releases of ERA will be posted on the support forum for download.

Running ERA

To run ERA, choose the Ubuntu icon in the top-left corner of the desktop and type “ERA”; the icon should appear in the “Applications” section.

SIDEKIQ NUC RF PORTS

NUC SMA Label	Sidekiq RF Ports	Software Handle
Rx	Rx1	skiq_rx_hdl_A1
Rx/Tx	Tx1/Rx2	skiq_tx_hdl_A1 / skiq_rx_hdl_A2
PPS	External 1 PPS Input	
REF	External 40 MHz REF Clock Input	

Table 9: *Sidekiq NUC RF Ports*

SIDEKIQ NUC GPIO CONNECTOR

The GPIO connector provides access to monitoring the power supply voltage and current to the mPCIe socket as well as providing access to lines used for digital I/O on the Sidekiq mPCIe. The ability to use a pin as GPIO depends on the loaded FPGA. The connector is a 2x8 header, 0.1" pin spacing, 0.025" square pins (standard size & spacing), Harwin P/N M20-9740846.

Function	Pin	Pin	Function
V_SENSE	1	2	**GND**
I_SENSE	3	4	**GND**
mPCIe pin 20	5	6	**N/C**

N/C	7	8	**N/C**
mPCIe pin 49	9	10	**mPCIe pin 47**
mPCIe pin 45	11	12	**mPCIe pin 46**
mPCIe pin 42	13	14	**mPCIe pin 44**
N/C	15	16	**GND**

Table 10: *Sidekiq NUC 8 GPIO*

V_SENSE: the voltage at the Sidekiq card. Nominally 3.3V.

I_SENSE: outputs a voltage proportional to current in volts/amp, i.e., 0.4 V means the Sidekiq card is drawing 400mA.

Function	Pin	Pin	Function
V_SENSE	1	2	**GND**
I_SENSE	3	4	**GND**
mPCIe pin 20	5	6	**GND**
N/C	7	8	**GND**
mPCIe pin 49	9	10	**mPCIe pin 47**
mPCIe pin 45	11	12	**mPCIe pin 46**
mPCIe pin 42	13	14	**mPCIe pin 44**
N/C	15	16	**GND**

Table 11: *Sidekiq NUC 11 GPIO*

V_SENSE: the voltage at the Sidekiq card. Nominally 3.3V.

I_SENSE: outputs a voltage proportional to current in volts/amp, i.e., 0.4 V means the Sidekiq card is drawing 400mA.

SIDEKIQ NUC JTAG CONNECTOR

The JTAG connector is a Samtec P/N STMM-107-02-G-D-RA. It will allow the standard Xilinx 14-pin JTAG cable to be attached.

Function	Pin	Pin	Function
N/C	1	2	**VREF***

GND	3	4	**TMS**
GND	5	6	**TCK**
GND	7	8	**TDO**
GND	9	10	**TDI**
GND	11	12	**N/C**
GND	13	14	**N/C**

***VREF** is a 2.5V output and establishes the required I/O voltage level for the JTAG adapter.

***Table 12:** Sidekiq NUC JTAG Connector*

ACCESSING SIDEKIQ NUC JTAG CONNECTOR

For customers adding their own custom FPGA blocks in the “user_app” area of the mPCIe Sidekiq reference design, it can often be useful to access JTAG to monitor signals in the FPGA through Xilinx's Chipscope software. The Sidekiq NUC PDK provides access to the Sidekiq’s JTAG port of the Xilinx Spartan-6 LX45T FPGA through a 2x7 header shown above. A standard Xilinx JTAG USB platform cable, such as the HW-USB-II-G, can be utilized to access JTAG on the FPGA.

Note: the default reference design does not have Chipscope ila instantiated and users will need to create a Chipscope ILA core through the gui ip core generator inside Vivado when building their custom design.

APPENDIX A – SIDEKIQ STATEMENT OF VOLATILITY

Model	mPCIe Sidekiq
Part Number	ES004-102
Manufacturer	Epiq Solutions
Address	3740 Industrial Avenue Rolling Meadows, IL 60008

Table 13: *Model, Part Number, and Manufacturer Info*

Memory Type	Memory Size	User Modifiable	Purpose	Process to Clear
On-Chip FPGA BRAM	2 Mb	Yes	Application usage	Power-off

Table 14: *mPCIe Sidekiq Volatile Memory*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
Flash	4 MB	Yes	No	Holds the FPGA bitstream	Cleared via API
EEPROM	16 KB	Yes	No	Contains product information for identifying the device (part#, serial#). User configuration settings (ref_clock). USB controller firmware	Product information and USB controller firmware are read only and must be returned to factory to be cleared. ref_clock setting is read/write via the API.

Table 15: *mPCIe Sidekiq Non-Volatile Memory*

APPENDIX B – FAILURE RATE & MTBF

Listed below are the failure rates and MTBFs for the ES004-200-C Sidekiq MPCIE 001 and ES004-205-C Sidekiq MPCIE 002 assemblies.

The calculations are derived from Relyence Reliability Software and based off a fixed/ground/controlled operating environment with an ambient temperature of 25°C.

Part Number	ES004-200-C
Description	Sidekiq MPCIE 001
Failure Rate (fpmh)	1.600783
MTBF (hours)	624694.32
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 16: *Sidekiq MPCIE 001 Failure Rate & MTBF*

Part Number	ES004-205-C
Description	Sidekiq MPCIE 002
Failure Rate (fpmh)	1.591310
MTBF (hours)	628413.02
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 17: *Sidekiq MPCIE 002 Failure Rate & MTBF*

[1] Software control of the reference clock setting via EEPROM setting is supported starting with Revision C of Sidekiq. Previous hardware revisions require a hardware modification to switch between internal and external reference clocks. Please contact Epiq Solutions for details.