Sidekiq™ M.2

RF Transceiver • Low SWaP

HARDWARE USER MANUAL

V1.5 - NOVEMBER 10, 2021

CHANGELOG

Revision	Date	Description	Author
0.1	2014-04-07	Pre-release draft, initial version	Barry L
0.3	2016-07-04	Completed all sections of document	Barry L
0.4	2016-07-08	Updated with Rev B hardware details/images	Barry L
0.5	2016-07-13	Updated with dimensioned mechanical drawings	Barry L
0.6	2016-08-07	Updated M.2 pinout table -Updated annotated I/O diagram	Barry L
0.7	2016-11-25	Corrected Figure 3 to show the proper PPS and GPIO I/O allocation -Added component temperature rating in 8.3 -Added details on thermal management recommendations in 9.11 and 10.4 -Added section 10.6 to clarify use of internal vs external reference clocks -Added details for Rev C of hardware: -Enumeration of TDD-capable RF antenna connectors -Updated M.2 edge connector pinout -Support for both Key B and Key M	Barry L
0.8	2017-11-02	Added section 10.7 on maximum acceptable Rx input power levels -Updated power consumption numbers	Barry L
0.9	2018-05-11	Added section 12 accelerometer axis orientation & temp sensor location, device part numbers -Added nominal tolerance of the 3.3V rail to section 10.3 -Added Rev C maximum recommended signal level of 3.3V to section 9.7 External PPS Input and section 9.9 FPGA GPIO#1 -Added libsidekiq handles / RF port mapping information to sections 9.1 – 9.4. -Updated table 3 input level 0dBm -Updated section 8.2 Gain Control Range -Added Port Mapping Table 7 -Removed Appendix A (empty)	Barry L
1.0	2018-07-12	Replaced rev b with rev c pics -Added links to section 5 & updated section 6 -Updated URLs & added hyperlinks -Updated sections 10.1.3 & 10.5 Windows OS support -Updated section 10.1.4 FPGA boot flash programing time over PCIe -Moved section 12 content to section 9.3 -Added Appendix A & B	Barry L
1.1	2020-01-02	Updated Appendix B and section 9.9	Barry L
1.2	2020-03-04	Added Appendix C, section 12, updated Appendix B	Barry L
1.3	2020-09-04	Markdown conversion	Barry L
1.4	2020-11-10	table updates and format cleanup	Barry L
1.5	2021-11-10	added NUC 8 and NUC 11 GPIO tables, format cleanup	Barry L

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INTRODUCTION

This document provides an overview of Epiq Solutions' Sidekiq M.2 SDR [1], an M.2 card with integrated RF transceiver, FPGA, and PCIe/USB interfaces to a host. This card is similar in concept to the original Sidekiq MiniPCIe card developed by Epiq Solutions, while complying with the new M.2 card specification. Sidekiq M.2 also provides enhanced capabilities to help customers perform more advanced radio signal processing. The following topics will be discussed:

- Overview of the Sidekiq M.2 hardware interfaces
- Sidekiq M.2 usage/integration options
- Sidekiq M.2 JTAG breakout board usage

All documentation and support for Sidekiq M.2 is provided through Epiq Solutions' support website which can be found at: support.epiqsolutions.com

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq M.2 is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. Each user of Sidekiq M.2 and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

Each Sidekiq M.2 unit is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq M.2 unit can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq M.2 from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation – A max input of -10 dBm is recommended
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

OVERVIEW

This guide provides an overview of the Sidekiq M.2 software defined radio hardware platform, associated capabilities, and basic usage. This includes the following:

- System level block diagram of the platform
- Overview of the externally accessible hardware ports
- Powering the system up and down

All documentation and support for Sidekiq M.2 is provided through Epiq Solutions' website:

Sidekiq M.2 Documentation

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

REFERENCES

1. **Sidekiq Product Page**

   epiqsolutions.com/rf-transceiver/sidekiq
2. **Epiq Solutions Support Page**

   support.epiqsolutions.com
3. **Berquist Thermal Gap Pad Material**

   https://www.bergquistcompany.com/thermal_materials/gap-pad.htm
4. **PCI-SIG PCIe M.2 Specifications**

   https://pcisig.com/specifications/pciexpress/

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
COTS	Commercial Off The Shelf
D/A	Digital to Analog converter
dB	Decibel
dBm	Decibels referenced to one milliwatt (mW)
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
GHz	gigaherz
GPIO	General Purpose Input / Output (I/O)
GPS	Global Positioning System
HSC	Murata brand of micro-miniature RF coax connector, manufactured for use as the antenna interface on M.2 cards
IF	Intermediate Frequency
I/Q	In-Phase / Quadrature Phase
JTAG	Joint Test Action Group
kHz	kilohertz
LED	Light Emitting Diode
MHF4	Micro miniature RF coax connector, manufactured for use as the antenna interface on M.2 cards
MHz	megahertz
MIMO	Multiple Input Multiple Output
ms	millisecond
PDK	Platform Development Kit
PPS	Pulse Per Second
PPM	Parts Per Million
RF	Radio Frequency
Rx	Receive
SDK	Software Development Kit
SDR	Software Defined Radio
TCVCXO	Temperature Compensated Voltage Controlled Crystal Oscillator

TDD	Time-division duplex
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
W.FL	Micro-Miniature RF coaxial connector manufactured by Hirose

Table 1: *Terms and Definitions*

SYSTEM OVERVIEW

Sidekiq M.2 is a miniature software defined radio card in a 3042 M.2 card form factor, providing a flexible wideband RF transceiver that can be used by a host system. The M.2 form factor is being adopted as the standard add-on card form factor for commercial tablets and laptops, where physical volume is aggressively being minimized. The features of the platform include the following:

- Compliant with M.2 3042-D3-B card form factor (30mm x 42mm x 4mm), Module Key B/M, Socket 2 (Note: Key M was added to the card starting with Rev C)
- RF transceiver covering 70 MHz to 6 GHz, with independent Tx and Rx frequencies (Analog Devices AD936x RFIC)
- Supports RF channel bandwidths up to 50 MHz
- Supports either 1x1 or 2x2 MIMO operation (depends on model; see product table below)
- A/D and D/A quadrature sample rates from 200 Ksamples/sec up to 61.44 Msamples/sec, with 12-bit precision
- User programmable FPGA for signal processing applications (Xilinx Artix XC7A50T-2CPG236I)
- SPI flash for storage and automatic FPGA bitstream loading at boot-up (Micron N25Q064A11EF640E or equivalent)
- On-board 40 MHz TCVCXO with +/- 1PPM accuracy; support for optional external 40 MHz reference clock input
- 8051-compatible microcontroller providing a USB 2.0 high speed interface to the host platform (Cypress FX2-based CY7C68053)
- PCIe Gen 2.0 (5 Gbps) x1 interface to the host platform
- Support for external 1PPS input signal for sample time alignment across multiple Sidekiq units
- Weight: 6 grams
- Power: ~2 W (application dependent)

Figure 1: *Sidekiq M.2 front side and back side*

To accommodate different applications, there are multiple variants of Sidekiq available to customers. These variants provide options for the number of Tx and Rx interfaces available, as well as how the PCIe transport interface is accessed, since certain host platforms may not include the PCIe signals at the edge connector. The following model table defines the different part numbers and their associated options. In addition, the Basic Usage in a Host System section provides additional detailed information on these options.

Epiq Solutions Part #	Description	Typical Usage
ES014-101	Supports 1Rx + 1Tx (1x1), with USB 2.0 and PCIe routed to edge connector per M.2 standard. This corresponds to a “-002” Sidekiq card as defined by the libsidekiq API.	Custom M.2 carriers where PCIe is guaranteed to be available on the edge connectors-Commercial platforms where PCIe has been verified to be present on the edge connector.
ES014-102	Supports 1Rx + 1Tx (1x1), with USB 2.0 routed to the edge connector per M.2 standard, and PCIe routed to low profile board connector for external access. This corresponds to a “-002” Sidekiq card as defined by the libsidekiq API.	Commercial platforms that include a 3042 M.2 slot with only USB 2.0 wired up, along with a 2230 M.2 slot with PCIe wired up (i.e., typical of WiFi M.2 cards).

ES014-103	Supports 2Rx + 2Tx (2x2 MIMO), with USB 2.0 and PCIe routed to edge connector per M.2 standard. This corresponds to a “-001” Sidekiq card as defined by the libsidekiq API.	Custom M.2 carriers where PCIe is guaranteed to be available on the edge connectors-Commercial platforms where PCIe has been verified to be present on the edge connector.
ES014-104	Supports 2Rx + 2Tx (2x2 MIMO), with USB 2.0 routed to the edge connector per M.2 standard, and PCIe routed to low profile board connector for external access. This corresponds to a “-001” Sidekiq card as defined by the libsidekiq API.	Commercial platforms that include a 3042 M.2 slot with only USB 2.0 wired up, along with a 2230 M.2 slot with PCIe wired up (i.e., typical of WiFi M.2 cards).

Table 2: *Breakdown of different Sidekiq M.2 card variants*

For the purposes of this document, the remaining documentation will be in reference to the 2x2 variant of Sidekiq M.2. A block diagram of Sidekiq M.2 is shown below.

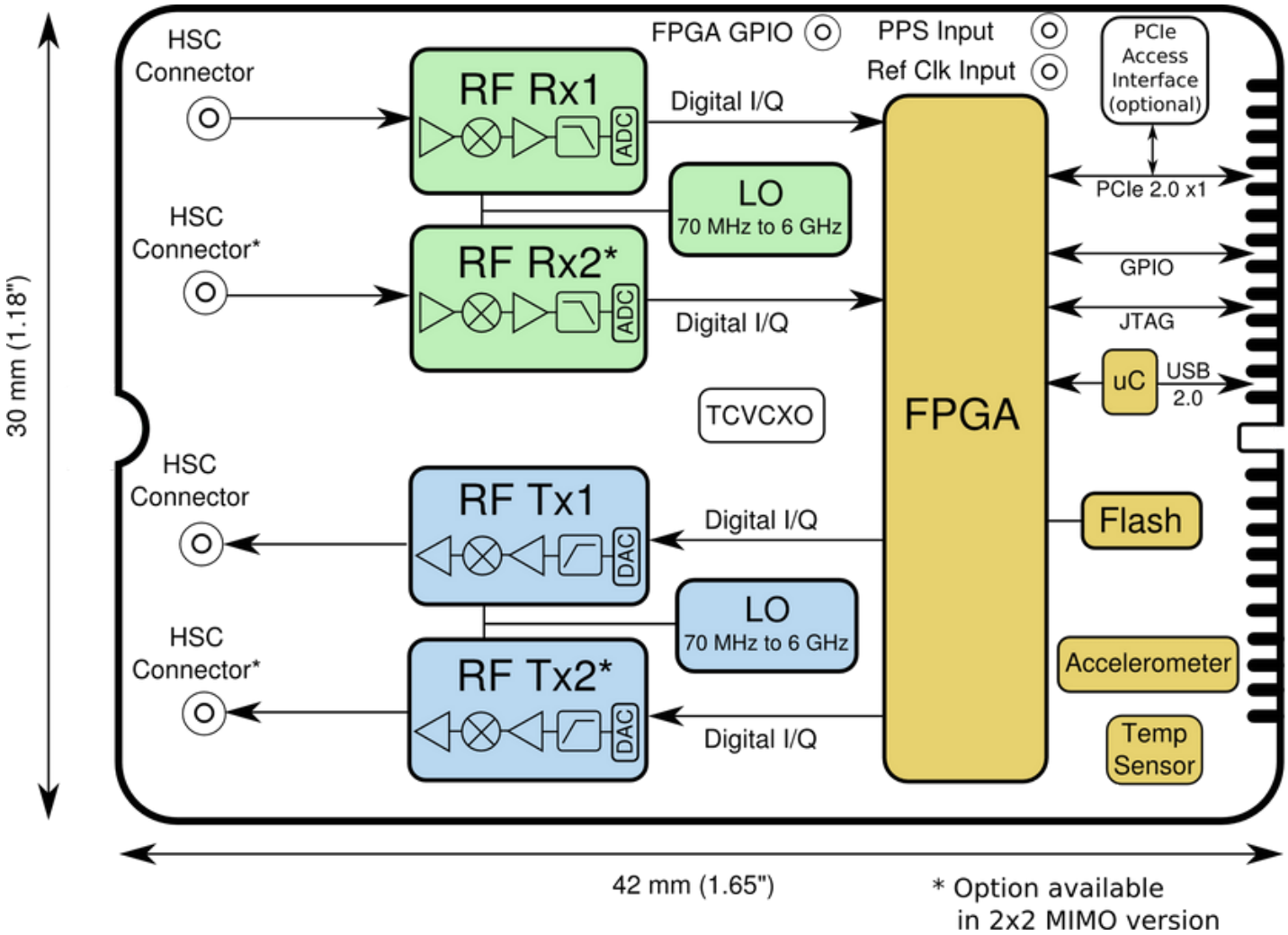

Figure 2: *Sidekiq M.2 block diagram*

HARDWARE SPECIFICATION

RF RECEIVER SPECIFICATION

RF Input	HSC miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	70 MHz to 6 GHz
Tuning Step Size	~2.4 Hz
Tuning Time	~1 ms
Typical Noise Figure	4-6 dB below 3 GHz, 6-9 dB from 3 GHz to 6 GHz
Typical IIP3	-10 dBm
Gain Control Range	0 to 76 dB, 1 dB steps
A/D Converter Sample Rate	200 Ksamples/sec to 61.44 Msamples/sec
A/D Converter Sample Width	12 bits
Typical I/Q balance	> 60 dB
On-board Reference Clock	40 MHz, +/- 1PPM accuracy (shared with Tx)

Table 3: *RF Receiver Spec*

RF TRANSMITTER SPECIFICATION

RF Input	HSC miniature coaxial connector (50 ohms)
Architecture	Zero-IF (direct conversion)
Tuning Range	70 MHz to 6 GHz
Tuning Step Size	~2.4 Hz
Tuning Time	~1 ms
Gain Control Range	0 to 89.75 dB, 0.25 dB steps
RF Output Power	+13 dBm < 2 GHz, +10 dBm above 2 GHz
D/A Converter Sample Rate	200 Ksamples/sec to 61.44 Msamples/sec
D/A Converter Sample Width	12 bits
Typical I/Q balance	> 60 dB

On-board Reference Clock	40 MHz, +/- 1PPM accuracy (shared with Rx)

Table 4: *RF Transmitter Spec*

HARDWARE SPECIFICATION

M.2 slot type	3042-D3-B/M card form factor (30mm x 42mm x 4mm), Module Key B/M, Socket 2
FPGA	Xilinx Artix 7 XC7A50T-2CPG236I with x1 PCIe interface to host
USB	Cypress FX2 microcontroller (CY7C68053) with USB 2.0 high-speed interface to host
FPGA Reprogramming	Over USB and PCIe
Accelerometer	3-axis
Temperature Sensor	-55 deg C to +125 deg C (+/- 2 deg C resolution)
Component Temperature Rating	-30 deg C* to + 85 deg C *Operation down to -40 deg C is supported, though the TCVCXO will operate outside of the +/- 1PPM accuracy specification.

Table 5: *HW Spec*

HARDWARE INTERFACES

Sidekiq M.2 provides a variety of different hardware interfaces for use by an end user. Each of these hardware interfaces is shown and defined below.

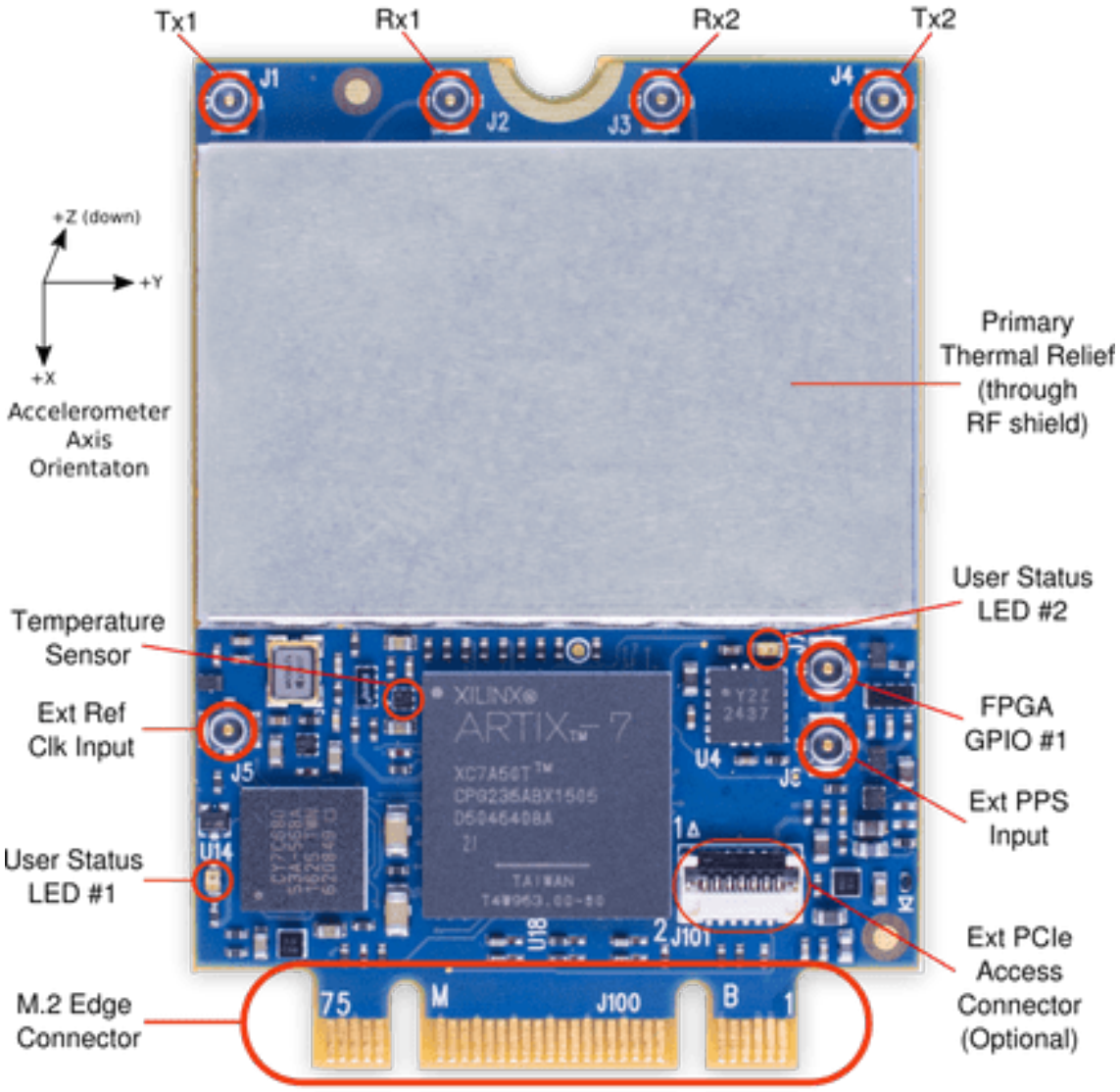

Figure 3: *Annotated diagram of Sidekiq M.2 hardware I/O interfaces*

TX1

The Tx1 interface is an HSC jack connector that provides an RF output path for the Tx1 antenna port in Sidekiq M.2. HSC is the standard interface utilized for the antenna interface on M.2 cards. This Tx port supports RF output frequencies between 70 MHz and 6 GHz. Note: HSC is similar to MHF4, but provides better mating with typical laptop antennas. These are both similar to, but not compatible with, W.FL. The libsidekiq software library TxA1 handle (sidekiq_tx_hdl_A1) is mapped to the Tx1 interface.

RX1

The Rx1 interface is a HSC jack connector that provides an RF input path for the Rx1 antenna port in Sidekiq M.2. HSC is the standard interface utilized for the antenna interface on M.2 cards. This Rx port supports RF input frequencies between 70 MHz and 6 GHz. Note 1: HSC is similar to MHF4, but provides better mating with typical laptop antennas. These are both similar to, but not compatible with, W.FL. Note 2: For TDD applications, this port can provide access to both Tx1 and Rx1, where the operating mode can be selected through software. The ability to switch between Tx and Rx on this antenna port is controlled from the FPGA, and is accessible via the libsidekiq software library. The libsidekiq software library RxA1 handle (sidekiq_rx_hdl_A1) is mapped to the Rx1 interface.

RX2

The Rx2 interface is a HSC jack connector that provides an RF input path for the Rx2 antenna port in Sidekiq M.2. HSC is the standard interface utilized for the antenna interface on M.2 cards. This Rx port supports RF input frequencies between 70 MHz and 6 GHz. Note 1: HSC is similar to MHF4, but provides better mating with typical laptop antennas. These are both similar to, but not compatible with, W.FL. Note 2: This antenna port is only utilized for Sidekiq M.2 variants that support 2x2 MIMO operation. Note 3: For TDD applications, this port can provide access to both Tx2 (sidekiq_tx_hdl_A2) and Rx2 (sidekiq_rx_hdl_A2), where the operating mode can be selected through software. The ability to switch between Tx and Rx on this antenna port is controlled from the FPGA, and is accessible via the libsidekiq software library. The libsidekiq software library RxA2 handle (sidekiq_rx_hdl_A2) is mapped to the Rx2 interface.

TX2

The Tx2 interface is a HSC jack connector that provides an RF output path for the Tx1 antenna port in Sidekiq M.2. HSC is the standard interface utilized for the antenna interface on M.2 cards. This Tx port supports RF output frequencies between 70 MHz and 6 GHz. Note 1: HSC is similar to MHF4, but provides better mating with typical laptop antennas. These are both similar to, but not compatible with, W.FL. Note 2: This antenna port is only utilized for Sidekiq M.2 variants that support 2x2 MIMO operation. The libsidekiq software library TxA2 handle (sidekiq_tx_hdl_A2) is mapped to the Tx2 interface.

Handle	RF Port [Fixed-Mode]	RF Port [TRX-Mode]
skiq_rx_hdl_A1	skiq_rf_port_J2	
skiq_rx_hdl_A2	skiq_rf_port_J3	
skiq_tx_hdl_A1	skiq_rf_port_J1	skiq_rf_port_J2
skiq_tx_hdl_A2	skiq_rf_port_J4	skiq_rf_port_J3

Table 6: *RF Port Mapping introduced in libsidekiq v4.6.0*

USER STATUS LED #1

The User LED #1 provides a visual status indicator that can be controlled through the libsidekiq software API. By default, this LED is used to provide an indication that the FPGA has successfully loaded and is running an FPGA bitstream.

USER STATUS LED #2

The User LED #2 provides a visual status indicator that can be controlled through the libsidekiq API. By default, this LED is used to provide an indication that a PCIe link has been successfully negotiated between the host CPU and the FPGA on Sidekiq. When this LED is illuminated, a PCIe link is being negotiated, and once the LED is no longer illuminated, a PCIe link has been established. During FPGA reprogramming, PCIe link is lost and then re-established after the bitstream has been successfully loaded.

EXTERNAL PPS INPUT

The External PPS Input interface is a HSC jack connector that allows an external PPS signal to be brought in to the on-board FPGA on Sidekiq for use in time synchronization. This signal on Rev B hardware is routed to the on-board FPGA through a 2.5V to 1.8V level shifter. A maximum recommended signal level of 2.5V can be applied to this input port, though this input port is 3.3V tolerant. Rev C hardware uses a 3.3V level shifter with a maximum recommended signal level of 3.3V applied to this input port. This PPS input is optional.

> **Note**: Since this signal is ultimately routed directly to the on-board FPGA, it is possible to also use this signal as a general purpose input/output. Contact Epiq Solutions for details of alternate usage of this port.

EXTERNAL REFERENCE CLOCK INPUT

The External Reference Clock Input interface is a HSC jack connector that allows an external 40 MHz reference clock to be brought in to Sidekiq and utilized instead of the default on-board 40 MHz TCVCXO. This provides the facility to have multiple Sidekiq cards share a common external 40 MHz reference clock. The selection between the on-board TCVCXO and an external 40 MHz reference clock is controlled through the libsidekiq software API.

The electrical specification for this input signal is defined below.

Input Level	0.8 – 1.3 Vpp, 0 dBm max from 50 ohm source
Input Impedance	AC-Coupled high impedance (10 Kohm || 10pF)
Frequency	40 MHz
Waveform	Square or Sinewave
Connector Type	HSC

Table 7: *Electrical specification for external reference clock input*

FPGA GPIO #1

The FPGA GPIO #1 interface is a HSC jack connector that provides access to a single FPGA GPIO pin on this micro coaxial connector. This allows for a digital single control signal from the FPGA to be accessed via a coaxial cable plugged in to this connector. Common uses for this would be to control an external RF switch, an enable/disable line for an RF power amplifier, etc.

This signal on Rev B hardware is routed to the on-board FPGA through a 2.5V to 1.8V level shifter. A maximum recommended signal level of 2.5V can be applied to this input port, though this input port is 3.3V tolerant.

Rev C hardware uses a 3.3V to 1.8V level shifter (TI TXB0102) with a maximum recommended signal level of 3.3V applied to this interface. When used as an input, the device driving this interface must have a drive strength of at least ±2 mA. When used as an output, the TXB0102 is designed to drive capacitive loads of up to 70 pF and has a low DC drive strength. If pullup or pulldown resistors are connected externally, the value must be kept higher than 50 kΩ to assure that it does not contend with the output drivers of the TXB0102.

EXTERNAL PCIE ACCESS CONNECTOR

The External PCIe Access Connector is used to provide an optional means to route signals related to PCIe from the host system to Sidekiq M.2. Ideally, the host platform adheres to the M.2 specification and has the PCIe signaling routed through the M.2 edge connector interface. However, many manufacturers of COTS computing platforms seem to omit the PCIe signals from the edge connector interface. If this is the case, the PCIe signals can be optionally accessed via this connector and an appropriate flex circuit to another device in the system where PCIe is accessible. Typically, this will be to a 2230 M.2 slot where PCIe is often available, and will require a custom card to be installed in the 2230 slot (such as Epiq Solutions' PCIe Access Card, part # ES014-210). See the Basic Usage in a Host System section for details of when this connector is typically used. Contact Epiq Solutions for flex circuit options.

Note that while the External PCIe Access Connector is populated on all Sidekiq M.2 cards, there are zero ohm resistors that must be properly installed for the PCIe signals to be routed to this connector. Otherwise, the PCIe signals are routed to the M.2 edge connector per the standard, and the External PCIe Access Connector is not utilized.

PRIMARY THERMAL RELIEF (RF SHIELD)

The RF shield (used to minimize the effects of RF noise entering the RF front end) serves as the primary thermal relief path for heat dissipation in the system. Underneath the shield, thermal gap pad material is used to transfer heat from components to the shield itself, yielding a minimal thermal resistance. If no air flow is available in the host system where Sidekiq M.2 is being integrated, it is highly recommended that the user provide a thermal dissipation path from this shield to a thermally conductive surface in the host system, such as a metal back plate or other metal housing. The use of thermal gap pad material can provide a flexible yet efficient thermal path between the RF shield and the host system.

In addition to the RF shield, the other primary component generating heat in Sidekiq M.2 is the Xilinx Artix 7 FPGA (which is located right next to the RF shield). If an end user is developing a thermal dissipation path for the RF shield, it is also recommended to include the FPGA in the thermal transfer path as well. Similar to the RF shield, use of a thermal gap pad material can be very effective in ensuring good thermal conductivity between this component and the host system.

SIDEKIQ ACCELEROMETER & TEMPERATURE SENSOR

The Sidekiq is equipped with temperature and accelerometer devices.

- Analog Devices 3-Axis Accelerometer ADXL346ACCZ
- Texas Instruments Temperature Sensor TMP103AYFFR

Please refer to the annotated diagram for the Sidekiq accelerometer axis orientation & temperature sensor location.

The libsidekiq software API provides access to these peripherals, test applications *read_accel* and *read_temp* are included with the sidekiq software. Additional information can be found in the Sidekiq Software Development manual.

M.2 EDGE CONNECTOR

The M.2 Edge Connector is used to route various signals between the M.2 host system and the Sidekiq card. Starting with Rev C, the Sidekiq M.2 card supports both Key B as well as Key M. A complete table enumerating the pins and their usage on Sidekiq M.2 Rev C is shown in the table below. For the previous Rev B hardware pinout (supporting only Key B), see the table in the External Reference Clock Input section. The primary pinout difference between Rev B and Rev C is the shuffling of GPIO signals to make room for the Key M key slot in the edge connector so that the card supports both Key B and Key M hosts.

Pin #	M.2 Pin Name	Description as used in Sidekiq M.2		Pin #	M.2 Pin Name	Description as used in Sidekiq M.2
1	CONFIG_3_	Unused (floating)		39	GND	Ground
2	+3.3V	+3.3V supply		40	GPIO0*	GPIO (FPGA pin G3), 1.8V
3	GND	Ground		41	PERN0	PCIe lane 0 host receiver diff pair (data module-->host)
4	+3.3V	+3.3V supply		42	GPIO1*	GPIO (FPGA pin J3), 1.8V
5	GND	Ground		43	PERP0	PCIe lane 0 host receiver diff pair (data module-->host)
6	FCPO#	Power down control		44	GPIO2*	GPIO (FPGA pin T17), 1.8V
7	USB_D+	USB D+ line		45	GND	Ground
8	W_DISABLE1#	Input only (FPGA pin J2), 3.3V tolerant		46	GPIO3*	GPIO (FPGA pin H2), 1.8V
9	USB_D-	USB D- line		47	PETN0	PCIe lane 0 host transmitter diff pair (data host-->module)
10	GPIO9	Unused (floating)		48	GPIO4	GPIO (FPGA pin T18), 1.8V
11	GND	Ground		49	PETP0	PCIe lane 0 host transmitter diff pair (data host-->module)
12	Key	N/A (Module B key)		50	PERST#	PCIe reset
13	Key	N/A (Module B key)		51	GND	Ground
14	Key	N/A (Module B key)		52	CLKREQ#	Clock Request, pulled low whenever Sidekiq M.2 is powered up
15	Key	N/A (Module B key)		53	REFCLKN	PCIe reference clock negative leg of diff pair, from host
16	Key	N/A (Module B key)		54	PEWAKE#	Unused (floating)
17	Key	N/A (Module B key)		55	REFCLKP	PCIe reference clock positive leg of diff pair, from host
18	Key	N/A (Module B key)		56	N/C	Pull low to enable JTAG I/O buffers

19	Key	N/A (Module B key)	57	GND	Ground
20	GPIO5**	GPIO/PPS input (FPGA pin N3), 1.8V signal, also connects to J6 connector through a 3.3V level shifter	58	N/C	Pull high to enable JTAG I/O buffers
21	CONFIG_0	Unused (floating)	59	Key	N/A (Module M key)
22	GPIO6	RFIC_SYNC / FPGA pin A16 (via 1 Mohm resistor), 1.8V signal	60	Key	N/A (Module M key)
23	GPIO11	Unused (floating)	61	Key	N/A (Module M key)
24	GPIO7	GPIO (FPGA pin J18), 1.8V	62	Key	N/A (Module M key)
25	DPR	Unused (floating)	63	Key	N/A (Module M key)
26	GPIO10	Unused (floating)	64	Key	N/A (Module M key)
27	GND	Ground	65	Key	N/A (Module M key)
28	GPIO8	Unused (floating)	66	Key	N/A (Module M key)
29	PERN1	Unused (floating)	67	RESET#	1.8V I/O, hard reset when low
30	UIM-RESET	JTAG TMS line for FPGA	68	SUSCLK	Unused (floating)
31	PERP1	Unused (floating)	69	CONFIG_1	Unused (floating)
32	UIM-CLK	JTAG TDO line for FPGA	70	3.3V	3.3V from host to power card
33	GND	Ground	71	GND	Ground
34	UIM-DATA	JTAG TDI line for FPGA	72	3.3V	3.3V from host to power card
35	PETN1	Unused (floating)	73	GND	Ground
36	UIM-PWR	JTAG TCK line for FPGA	74	3.3V	3.3V from host to power card
37	PETP1	Unused (floating)	75	CONFIG_2	Pulled low through resistor to ground

38	DEVSLP	Unused (floating)		76	N/C	Unused (floating)

Table 8: *Sidekiq M.2 edge connector signal descriptions for Rev C hardware*

* This indicates a GPIO pin that is preferred for use when interfacing to a custom host platform. These pins will receive priority in terms of GPIO backward compatibility if future variants of Sidekiq require changes to the GPIO allocation.

** This GPIO pin is preferred for receiving a PPS input signal from the host platform.

BASIC USAGE IN A HOST SYSTEM

HOST SYSTEM COMPATIBILITY

From a hardware perspective, Sidekiq M.2 is mechanically and electrically compatible with any host system that provides a standards-compliant 3042 Key B/M M.2 card slot. However, there are several points to note regarding the usage of Sidekiq M.2 in different host systems. The following section provides an overview of these details.

USB/PCIE SIGNAL AVAILABILITY IN HOST PLATFORM

Sidekiq M.2 utilizes a 3042-D3-B card form factor (30mm x 42mm x 4mm), Module Key B/M, Socket 2. It includes both PCIe Gen2 x1 signaling interface, as well as a USB 2.0 high speed interface, as defined in the PCI-SIG's M.2 card specification [4]. When interfacing Sidekiq M.2 to a host system, there are four different usage configurations available based on the electrical signaling interface provided by the host system.

Configuration #1: Custom Host Platform with both USB and PCIe Signals Available in the 3042 M.2 Slot

For users developing their own host platform for Sidekiq M.2, it is recommended to have both the USB 2.0 interface and the PCIe x1 interface wired up to provide maximum capability from the Sidekiq M.2 card. This will allow the PCIe interface to be used for high speed transport between the host and the card, where the Gen2 x1 interface on Sidekiq can support > 400 MB/sec. The USB 2.0 interface can then be used for fast FPGA re-programming. The recommended Sidekiq M.2 part number for use in this kind of system is either ES014-101 (for 1x1 Tx/Rx capability) or ES014-103 (for 2x2 MIMO capability).

Configuration #2: COTS Host Platform with both USB and PCIe Signals Available in the 3042 M.2 Slot

Usage of Sidekiq M.2 in a COTS host platform that includes both PCIe and USB 2.0 signaling is identical to Configuration #1 above. It should be noted that this configuration in a COTS host platform appears to be non-standard, and there is no definitive way to determine if a COTS host platform has both USB and PCIe signals available. Two example COTS host platforms with a 3042 M.2 slot that include both PCIe and USB signals are:

- Dell Precision 77x0 laptop
- Intel NUC model NUC5i5MYHE, NUC8I7BEH, NUC11TNHi5/i7, or later

Configuration #3: COTS Host Platform with only USB Signals Available in the 3042 M.2 Slot

The most common use case for including a 3042 M.2 slot in a COTS laptop or tablet platform is to allow a 2G/3G/4G cellular modem card to be installed in the system to access the internet via a cellular connection. The vast majority of these cellular modem cards only utilize the high speed USB 2.0 interface to communicate between the COTS laptop/tablet and the M.2 card, and thus the typical COTS laptop/tablet host platform leaves the PCIe interface signals unconnected on the host side in this M.2 slot.

If a user is interested in integrating a Sidekiq M.2 card into a COTS laptop/tablet, there is a high likelihood that the M.2 slot in the laptop/tablet will only have a high speed USB 2.0 interface wired up. Unfortunately, there is no simple way to determine whether both the USB 2.0 and PCIe signals are wired up in a slot, or if just the USB 2.0 signals are wired up. It is worth noting that most laptops only ensure that the USB 2.0 interface is available in the slot. If this is the case, the maximum data transport rate between the host system and the M.2 card will be approximately 30 MB/sec, due to the fact that USB 2.0 is substantially slower than PCIe.

For applications where only USB 2.0 high speed signaling will be used between the host and the Sidekiq M.2 card, the recommended Sidekiq M.2 part number for use in this kind of system is either ES014-101 (for 1x1 Tx/Rx capability) or ES014-103 (for 2x2 MIMO capability).

Configuration #4: COTS Host Platform with only USB Signals Available in the 3042 M.2 Slot, and PCIe Signals in a 2230 M.2 Slot

Many modern laptops include multiple M.2 slots. A common configuration is to include one 3042 M.2 card slot to support an embedded 2G/3G/4G cellular modem card, and a second smaller M.2 slot (2230 type, which measures 22mm x 30mm) to support a Wi-Fi card. While the 3042 M.2 slot in these laptops may not have PCIe signals wired in, the 2230 M.2 slot for the Wi-Fi card typically will have PCIe signals wired in, since the high data rates of modern Wi-Fi requires the faster transport capability of PCIe.

Epiq Solutions has developed a hybrid solution to allow a Sidekiq M.2 card to be installed in a 3042 slot (accessing both power and USB 2.0 from this slot), while also accessing the PCIe interface available in the 2230 M.2 slot. The solution requires a custom 2230 M.2 “PCIe access card” to be installed in the 2230 slot, with a flex circuit connecting the Sidekiq M.2 card to the PCIe access card. In this configuration, a Sidekiq M.2 card installed in to the 3042 slot can get access to the PCIe Gen2 interface provided by the 2230 slot, and thus provide fast data transport between the host and the card. Note that if a Wi-Fi card is already installed in the 2230 M.2 slot, this card will no longer be available to the user since the PCIe access card needs to be plugged in to this card slot.

Different host platforms may require different types of flex circuits based on the relative positioning of the 3042 M.2 slot to the 2230 M.2 slot. Epiq Solutions has developed several different flex circuit options that can be utilized here, and can work with customers to develop a solution that fits their specific needs.

The recommended Sidekiq M.2 part number for use in this kind of system is either ES014-102 (for 1x1 Tx/Rx capability) or ES014-104 (for 2x2 MIMO capability), where the PCIe interface is accessible via a small flex circuit connector instead of the standard edge launched M.2 pins. In addition, the part number for the 2230 M.2 PCIe access card is ES014-210.

BIOS COMPATIBILITY

Different host systems enforce different rules regarding which M.2 cards are considered to be compatible with their platform. In some cases, such as laptops manufactured by Lenovo, the BIOS of the computer may probe the M.2 slots to identify the type/manufacturer of the card installed at power-up. If the detected card is not in a pre-defined “white list” of compatible cards, the host system will not continue booting up. Other laptops, such as those manufactured by Dell, Inc., have no such restrictions. It is recommended that the end user verify whether or not their intended host system imposes any limitations regarding compatible cards.

OPERATING SYSTEM COMPATIBILITY

Windows 7 and 10 are currently supported. Windows 7 support was added in the Sidekiq SDK v4.4.0 release and Windows 10 support was added in the Sidekiq SDK v4.6.0 release.

Various Linux kernel versions have been tested starting at version 3.0. Sidekiq has been tested both in x86-based Linux systems as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported. Please contact Epiq Solutions for details.

For customers interested in doing a custom build of the Sidekiq PCIe device driver for their host platform, a license for the source code for this device driver is also available separately. Please contact Epiq Solutions for details.

FPGA RECONFIGURATION/REPROGRAMMING OPTIONS

The FPGA bitstream can be reconfigured at run-time with a new bitstream from the host system. This programming sequence utilizes the USB interface by default. This FPGA re-programming operation temporarily brings down the PCIe interface, and thus the PCIe interface can't be used during this time. The typical time required to reconfigure the FPGA with a new bitstream is ~3 seconds.

Alternately, for host systems that only have the PCIe interface (and no USB), support for re-programming the FPGA boot flash over PCIe is also provided. This can be followed by an FPGA reset operation to re-load the bitstream from flash. This allows new FPGA bitstreams to be programmed down and re-loaded only using the PCIe interface. Note, however, that this operation takes substantially longer than operating over USB (typically ~1 minute), due to the fact that the SPI boot flash used by the FPGA is being re-programmed.

RF INTERFACES

Many host systems that support M.2 come pre-wired with antennas already integrated in to the host system. These antennas typically terminate in HSC connectors, since this is the standard that is defined for use by M.2 cards. The range of RF frequencies supported by the antennas, as well as the gain of the antennas, will be platform specific. Typically, these internal antennas have support for cellular frequencies (700 MHz to 1 GHz, and 1700 MHz to 2.1 GHz), as well as Wi-Fi frequencies (2.4 GHz and 5.9 GHz), but it is up to the user to validate the performance of the antenna solution. Sidekiq M.2 has four HSC antenna ports which are compatible with antennas in the host system. By default, this allows for two Rx antennas and two Tx antennas to be connected to Sidekiq M.2. Starting with Rev C of the hardware, it is also possible to use a single antenna port for both Tx and Rx operations, controlled via software.

SYSTEM INTERFACE OPTIONS

Sidekiq can be interfaced to a host system through different electrical/physical interfaces. The following sections provide details of several potential options.

> **Note**: Sidekiq should never be inserted into or removed from a host system with power applied to the host system. This could permanently damage the card.

M.2 SLOT

The most common method for interfacing Sidekiq M.2 to a host system, such as a laptop or an embedded single board computer, is through a built-in M.2 slot in the host system. This provides the most compact interfacing option from a size perspective, though may require some level of dis-assembly of the host system to access the card slots.

MINIPCIE SLOT

For host systems that include a MiniPCIe slot, Epiq Solutions has developed an M.2-to-MiniPCIe adapter board (part number ES014-208) to allow Sidekiq M.2 to be used in MiniPCIe slots. This adapter board accepts a Sidekiq M.2 card, and connects all of the necessary signals between the M.2 edge connector and the MiniPCIe edge connector. With this configuration, the PCIe x1 Gen2 interface as well as the USB 2.0 interface can be fully utilized. Note: The two board stack up consisting of the M.2 plus the adapter board requires ~1.5 mm of additional height in the card slot. The figure below shows the two board stack of Sidekiq M.2 plus M.2-to-MiniPCIe adapter board.

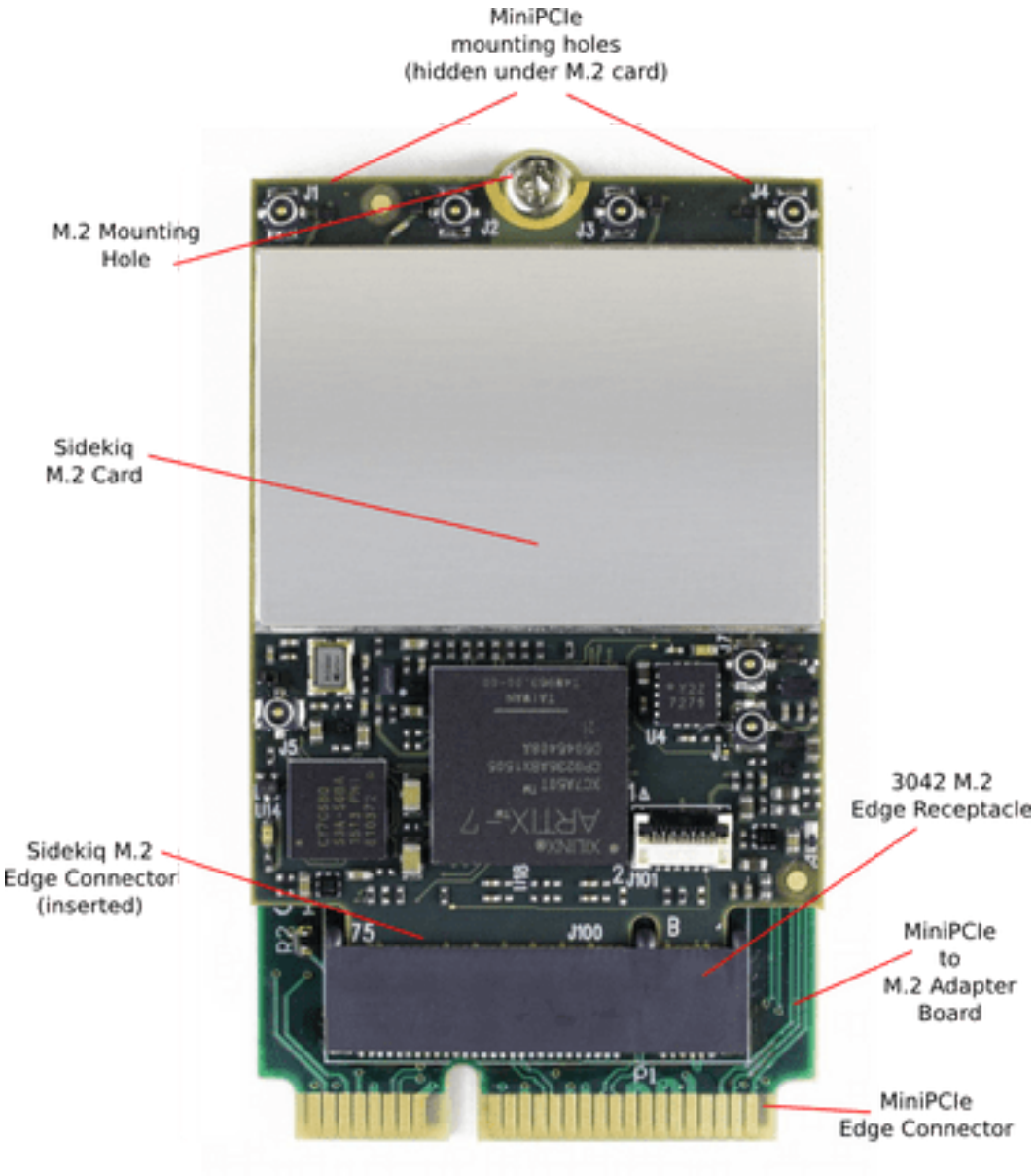

Figure 4: *Sidekiq M.2 inserted into Epiq Solutions' M.2-to-MiniPCIe adapter board*

PCIE SLOT

The majority of the computer motherboards manufactured today come with at least one standard PCIe expansion slot. These slots are typically used to add peripherals to the host computer, such as network cards etc. Several manufacturers make PCIe-to-M.2 (or PCIe-to-MiniPCIe) adapter cards that can be used to allow Sidekiq to interface to a host system's PCIe slot. These slots only provide the PCIe interface natively, so the USB interface is often broken out to a separate USB connector on the PCIe-to-MiniPCIe adapter card. This allows the user to plug a USB cable in between the adapter card and another available USB port in the host system.

POWER CONSUMPTION

The power consumption of Sidekiq M.2 varies depending on the configuration and application of the card. Host systems supporting M.2 typically provide a maximum of 3.5W of power on the 3.3V rail to each M.2 card, so this sets the upper bounds of what Sidekiq can consume. Nominal tolerance of the 3.3V rail is +/-9%.

The table below provides a listing of power consumption under different operating conditions. Note that each of these assumes that the stock Sidekiq M.2 FPGA reference design loaded in to the FPGA.

Test Scenario	Power Consumption (in Watts)
Test scenario #1: Card powered up but idle (no Tx or Rx)	1.36 W
Test scenario #2: Card powered up, single channel Rx tuned to 850 MHz streaming over PCIe at a sample rate of 30 Msamples/sec	2.23 W
Test scenario #3: Card powered up, single channel Rx tuned to 850 MHz streaming over PCIe at a sample rate of 30 Msamples/sec, single channel Tx tuned to 3.8 GHz (Tx attenuation=0) streaming over PCIe at a sample rate of 30 Msamples/sec	2.72 W

Table 9: *Example power consumption estimates for Sidekiq M.2*

THERMAL DISSIPATION

Effective use of Sidekiq M.2 in a system also requires consideration of an appropriate thermal dissipation solution. Since Sidekiq M.2 can be integrated into a variety of different host systems with different thermal profiles (i.e., forced air, natural convection, etc), the end user is required to perform their own system analysis to determine what level of thermal dissipation is appropriate for their use-case. Sidekiq M.2 uses components that are rated for operation to +85 deg C, and thus the end user must ensure that the temperature reported by the on-board temperature sensor does not exceed +85 deg C. **Exceeding the maximum rated temperature of +85 deg C may damage the Sidekiq M.2 card and/or accelerate failure of the card.**

As discussed in the Thermal Relief (RF Shield) section , both the RF shield as well as the FPGA are the two primary sources of heat requiring thermal dissipation. It is highly recommended that a thermal transfer solution, such as gap pad [3], be used to provide a thermal dissipation path between the RF shield/FPGA and an external conduction surface in the host system. With adequate thermal transfer to the host system, it is common for Sidekiq M.2 to report steady state board temperatures in the range of 55 deg C to 60 deg C while fully operational. Note: The actual temperature range achievable in a given system may vary substantially depending on a number of

factors, including the number of RF receivers operational, the number of RF transmitters operational, the A/D and D/A sample rates, customizations done to the FPGA, and others. Again, it is strongly recommended that a thorough system evaluation be performed by the customer to fully characterize the thermal profile of Sidekiq M.2 in their system. Please refer to the annotated diagram for the temperature sensor location.

PROPER DETECTION OF SIDEKIQ IN A HOST SYSTEM

A properly configured Windows host system (with the necessary device driver loaded) with both PCIe and USB 2.0 will allow Sidekiq M.2 to enumerate on both the PCIe bus as well as the USB bus.

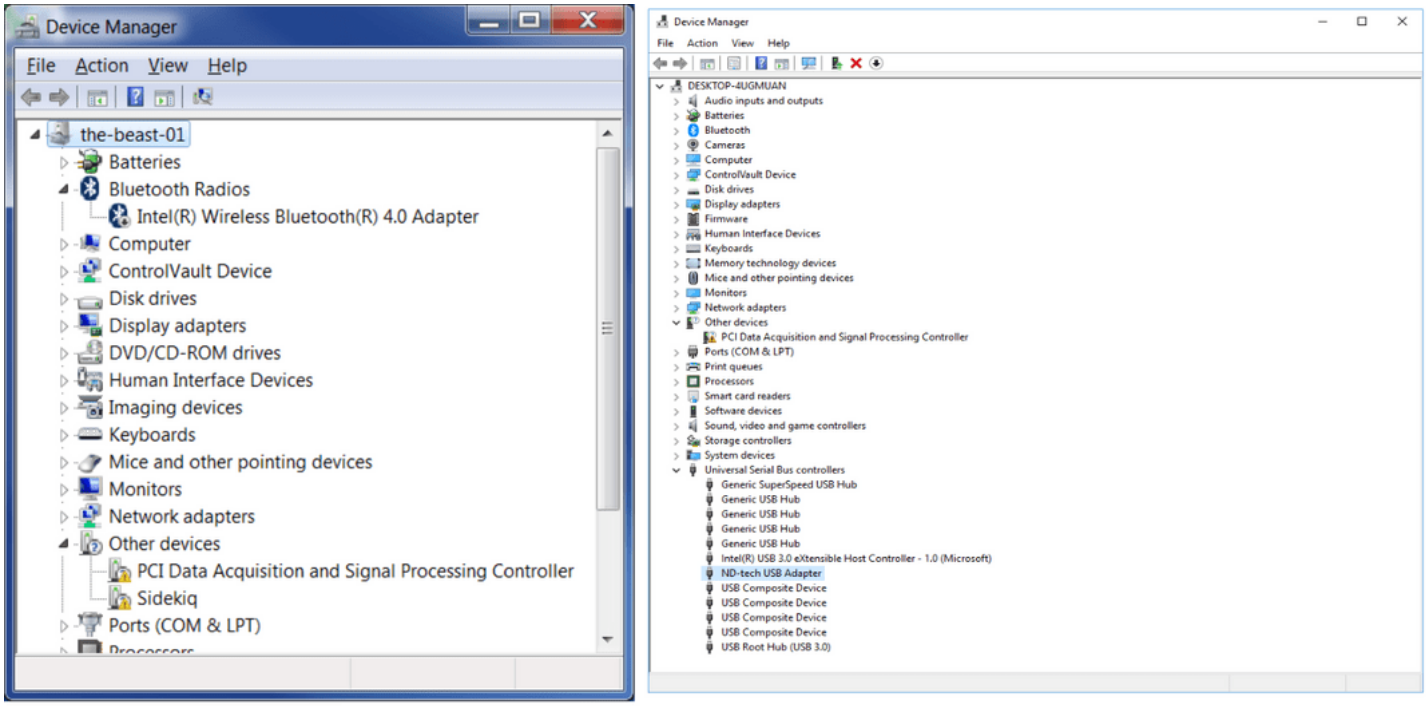

Figure 5: *Detection of Sidekiq in Windows 10*

Please refer to the Windows Sidekiq Development section of the Sidekiq Development Manual for additional information.

A properly configured Linux host system (with the necessary dmadriver.ko device driver loaded) with both PCIe and USB 2.0 will allow Sidekiq M.2 to enumerate on both the PCIe bus as well as the USB bus. The enumeration on the PCIe bus can be verified by executing the command “lspci” to confirm the presence of Sidekiq. The execution of “lspci” will provide output similar to the following when Sidekiq is detected (the detection of Sidekiq is in bold, and shows up as a “Signal processing controller”, negotiating to a Gen2 PCIe link at 5 Gbps:

...

00:1f.3 SMBus: Intel Corporation 7 Series/C210 Series Chipset Family SMBus Controller (rev 04)
02:00.0 Network controller: Broadcom Corporation BCM4313 802.11bgn Wireless Network Adapter (rev 01)
03:00.0 Signal processing controller: Device 19aa:7021 (rev 04)
0b:00.0 SD Host controller: O2 Micro, Inc. OZ600FJ0/OZ900FJ0/OZ600FJS SD/MMC Card Reader Controller (rev 05)
0c:00.0 Ethernet controller: Broadcom Corporation NetXtreme BCM5761 Gigabit Ethernet PCIe (rev 10)

...

Similarly, Sidekiq enumerates on the USB bus. This enumeration can be verified by executing the command “lsusb” to confirm the presence of Sidekiq. The execution of “sudo lsusb -v” will provide a verbose listing of all USB devices currently enumerated in the system, with output similar to the following when Sidekiq is detected:

...

Bus 001 Device 003: ID 04b4:1004 Cypress Semiconductor Corp.
Device Descriptor:
bLength18
bDescriptorType1
bcdUSB2.00
bDeviceClass0 (Defined at Interface level)
bDeviceSubClass0
bDeviceProtocol0
bMaxPacketSize064
idVendor0x04b4 Cypress Semiconductor Corp.
idProduct0x1004
bcdDevice0.00
iManufacturer1 Epiq Solutions
iProduct2 Sidekiq

...

INTERNAL/EXTERNAL REFERENCE CLOCK OPTIONS

Sidekiq M.2 supports options to use either an internal (i.e. on-board) 40 MHz TCVCXO as a reference clock, or an external 40 MHz reference clock as defined in External Reference Clock Input section. Regardless of which clock source is selected, this clock serves as the reference for both the RF front end as well as the digital processing blocks in the FPGA. The selection of whether Sidekiq

M.2 uses the internal reference clock or the external reference clock is stored as a configuration parameter in EEPROM on the card. This parameter is read by a microcontroller on-board Sidekiq at power-up, and is used to configure how the card should operate.

If Sidekiq is configured to use an external reference clock, but no external reference clock is provided via the HSC connecton, any application attempting to initialize the Sidekiq card will fail.

For cases where a customer would like to switch between internal and external reference clock options, a software application can be provided to update the EEPROM configuration settings. Please contact Epiq Solutions for details.

For cases where an alternate external reference clock frequency are of interest (besides 40 MHz), additional frequencies may be supported. Please contact Epiq Solutions for details.

MAXIMUM RF POWER INPUT AT RF INPUT CONNECTOR

It is often necessary for the system integrator to understand the maximum RF input signal that can be received by Sidekiq M.2. The maximum acceptable RF power input at the Rx HSC connector depends on the operating mode of the card:

- If the RF receiver is tuned <= 3 GHz (which uses the “low band” Rx path), and RF input signals are being received below 3 GHz, the maximum allowable RF input power level at the HSC Rx connector without causing damage is +23 dBm. Note: An RF overload protection circuit automatically engages when the RF input power level reaches approximately -8 dBm to protect the hardware up until the +23 dBm input level.
- If the RF receiver is tuned > 3 GHz (which uses the “high band” Rx path), and RF input signals are being received > 2 GHz, the maximum allowable RF input power level at the HSC Rx connector without causing damage is -8 dBm. Note: The “high band” Rx path does not have any RF overload protection circuitry in-line due to space constraints. Further, there is an LNA to increase the Rx sensitivity up to 6 GHz.
- If the RF receiver is tuned > 3 GHz (which uses the “high band” Rx path), and RF input signals are being received <= 2 GHz, the maximum allowable RF input power level at the HSC Rx connector without causing damage is +12 dBm. Note: The 3 GHz high pass filter in-line with the “high band” Rx path provides the extra signal attenuation to increase the maximum allowed RF input signal under these conditions.

SUPPORT FOR HOST SYSTEM SLEEP/HIBERNATION

Some host systems that have a “sleep mode” or “hibernation” mode where power is no longer applied to the M.2 slot while in this state. Sidekiq does not currently have proper support to handle these transitions, since the FPGA bitstream would be lost during this transition. Thus, if the host system enters in to a sleep/hibernation state, it should be assumed that the Sidekiq M.2 card will likely need to undergo a complete reboot in order to fully use all features of the card again. For example, if a Sidekiq M.2 card is installed in a laptop with power savings mode enabled each time the laptop lid closes, proper Sidekiq operation is not guaranteed after the laptop lid is re-opened.

JTAG ACCESS ON SIDEKIQ

The Xilinx Artix 7 XC7A50T FPGA utilized on Sidekiq M.2 provides a JTAG interface that can be accessed and utilized during the development of custom logic/processing modules targeting the FPGA. However, due to size constraints, there is no space available on Sidekiq M.2 for a standard JTAG interface. Thus, the JTAG interface signals are routed to the M.2 edge connector (see Table 5 for pinout details). Due to the fact that no host system would typically route these signals to a JTAG header, Epiq Solutions developed a stand-alone JTAG adapter card to provide access to these JTAG signals. In this configuration, Sidekiq that can be used in conjunction with an M.2 extender ribbon cable to connect the M.2 signals to the host system through the M.2 extender card. This allows standard FPGA JTAG programmers/debuggers, such as the Xilinx Platform USB Cable II, and the Digilent HS2 1x5 JTAG debug pod, to be used with Sidekiq M.2. Figure 6 shows Sidekiq installed in the JTAG Board, with the associated M.2 adapter card that can be installed in the host system. Note: No additional power source is required for the Sidekiq JTAG board. Power is derived from the host system, through the 3.3V interface provided by the M.2 connector.

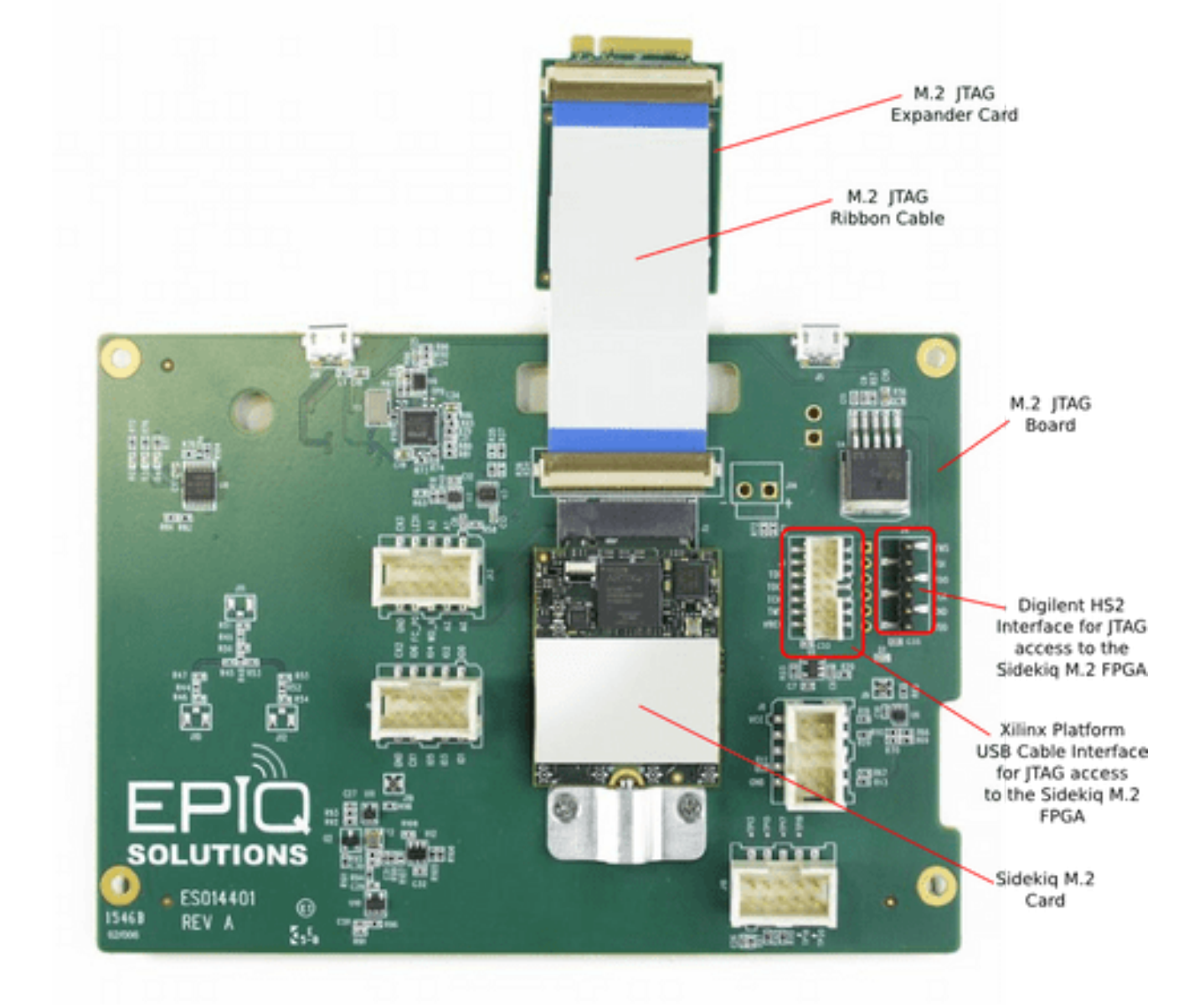

Figure 6: *Sidekiq M.2 JTAG Board plus M.2 adapter card for use in debugging*

The Sidekiq M.2 JTAG board provides several additional interfaces that can be used for testing Sidekiq, such as power consumption measurement and access to the FPGA GPIO signals provided by Sidekiq at the M.2 edge connector. Contact Epiq Solutions for additional details of these features.

JTAG BOARD USAGE NOTES

The following section provides usage notes for the Sidekiq M.2 JTAG Board.

- Details of using Xilinx tools to program and debug FPGA bitstreams with Sidekiq can be found in the Sidekiq FPGA Developer's Manual [1].
- The Sidekiq JTAG Board is powered through the M.2 interface, with power coming from the host system. No additional power supply is required for the JTAG Board.
- Only one JTAG pod should be connected to the JTAG Board at any given time. Plugging in a JTAG pod to both JTAG interfaces will damage the JTAG Board.

- The signal integrity of the M.2 JTAG Ribbon Cable has been tested in several different systems without any issues. Longer ribbon cables may also work, though it is up to the end user to verify functionality.

SIDEKIQ M.2 MECHANICAL OUTLINE

A dimensioned mechanical drawing of Sidekiq M.2 is shown in the figure below. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.

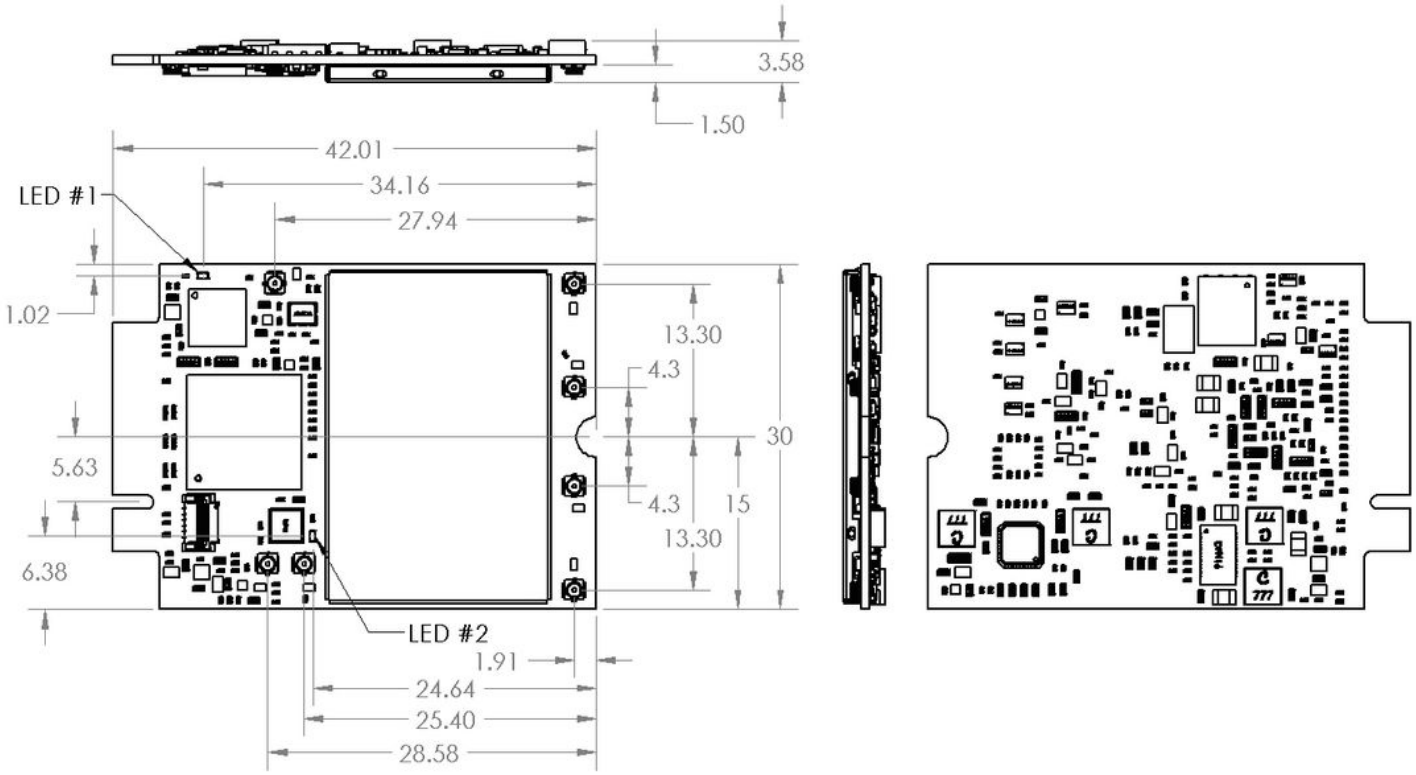

Figure 7: *Sidekiq M.2 Mechanical Outline*

SIDEKIQ M.2 NUC PLATFORM DEVELOPMENT KIT (PDK)

SIDEKIQ M.2 NUC PDK OVERVIEW

The Sidekiq M.2 NUC PDK includes one Sidekiq M.2 card hosted on an Intel NUC8I7BEH, NUC11TNHi5/i7, or later Mini PC NUC system.

The Sidekiq M.2 NUC PDK is pre-loaded with Epiq Solutions' libsidekiq API, test applications, ERA (Spectrum Analyzer), and device drivers. All support-related questions, product documentation, software, and FPGA reference designs are managed through Epiq Solutions' private web-based support forum* available at epiqsolutions.com/support.

*Registration is required to use the Epiq Solutions Customer Support Center. You can register at epiqsolutions.com/support

Figure 8: *Sidekiq M.2 NUC hardware I/O interfaces*

Figure 9: *More Sidekiq M.2 NUC hardware I/O interfaces*

SIDEKIQ M.2 NUC PDK SETUP

After you have removed all of the package contents, setup the system as follows:

1. Connect a USB keyboard, mouse to available USB ports, HDMI monitor to HDMI port, a network cable to the RJ45 port, and the DC power supply cable from the provided DC power brick.
2. Connect an antenna or RF source to RX SMA before using any of the test applications or ERA; for more details, see “Sidekiq M.2 NUC RF Ports” below.
3. Power on the NUC; this will also power-on the connected TB3 chassis. The computer monitor will indicate that it is starting up Ubuntu Linux and then it will show a login page.
4. Log into Ubuntu with the user credentials:
5. Username: **sidekiq**
6. Password: **sidekiq**

INCLUDED APPLICATIONS

Several applications are included with the PDK in order to help you test and verify your setup, such as our standard Sidekiq command-line test applications and ERA, a spectrum analyzer.

Libsidekiq Test Applications are located in: */home/sidekiq/sidekiq_image_current/test_apps*.

Launch a terminal window from Dash (search for “Terminal”) or by pressing Ctrl-Alt-T.

```
cd /home/sidekiq/sidekiq_image_current/test_apps/
```

A user can scan the system for Sidekiq cards, displaying version information for one or all card(s) upon detection by running the **version_test** application by executing the command:

./version_test

The application should return results that look something like the following:

```
$ ./version_test
SKIQ[4586]: <INFO> Need to perform full initialization
SKIQ[4586]: <INFO> Performing detection of cards
SKIQ[4586]: <INFO> Sidekiq card detection completed successfully!
SKIQ[4586]: <INFO> Preliminary initialization complete, continue full initialization
1 card(s) found: 0 in use, 1 available!
Card IDs currently used     :
Card IDs currently available: 0
Info: initializing 1 card(s)...
SKIQ[4586]: <INFO> libsidekiq v4.13.0 (g0c87aa729)
version_test[4586]: <INFO> Sidekiq card 0 is serial number=####, hardware M2 C (rev C), product
SKIQ-M2-001 (M.2) (part ES01420*-C0-00)
version_test[4586]: <INFO> Sidekiq card 0 firmware v2.9
version_test[4586]: <INFO> Sidekiq card 0 FPGA v3.13.1, (date 20060820, FIFO size 16k)
version_test[4586]: <INFO> Sidekiq card 0 is configured for an internal reference clock
version_test[4586]: <INFO> Loading calibration data for Sidekiq M.2, card 0
**********************************************************
* libsidekiq v4.13.0
**********************************************************
**********************************************************
* Sidekiq Card 0
  Card
    accelerometer present: true
    part type: M.2
    part info: ES01420*-C0-00
    serial: ####
    xport: PCIe
  FPGA
    version: 3.13.1
    git hash: 0x043ec0e2
    build date (yymmddhh): 20060820
    tx fifo size: 16k samples
  FW
    version: 2.9
  RF
    reference clock: internal
    reference clock frequency: 40000000 Hz

version_test[4586]: <INFO> Unlocking card 0
```

Raw I/Q Capture

A user can perform an RF capture of I/Q samples using the default configuration by executing the **rx_samples** application as follows:

```
./rx_samples -c 0 --handle=A1 -r 30.72e6 -b 25e6 -f 1e9 -d /tmp/out
```

This command will save I/Q samples to a file named /tmp/out.a1 using values for 30.72 Msps sample rate, 25 MHz channel bandwidth, 1 GHz tune frequency. The data is stored in the file as 16-bit I/Q pairs with 'I' samples stored in the upper 16-bits of each word, and 'Q' samples stored in the lower 16-bits of each** word. **Additional available options are described by executing:

```
./rx_samples -h
```

ERA - Epiq RF Analyzer

EPIQ RF Analyzer (ERA) is installed on the Sidekiq M.2 NUC PDK. ERA is an application that controls an Epiq radio and provides a realtime view of spectrum, radio frequency, sample rate, and filtering configuration.

ERA Release Information

- The included version does not provide "Pro" features of ERA for (e.g. recording, see User Manual for all Pro-only features). Future releases of ERA will be posted on the support forum for download.

Running ERA

To run ERA, choose the Ubuntu icon in the top-left corner of the desktop and type "ERA"; the icon should appear in the "Applications" section.

Note: The ERA User's manual is available on the support forum https://support.epiqsolutions.com/viewforum.php?f=358 and provides instructions on the features and operation of ERA; some of these features described in the manual require the purchase of an ERA Pro license.

SIDEKIQ M.2 NUC RF PORTS

NUC SMA Label	Sidekiq RF Ports	Software Handle
Rx1	Rx1	skiq_rx_hdl_A1
Rx2	Rx2	skiq_rx_hdl_A2
Tx1	Tx1	skiq_tx_hdl_A1
Tx2	Tx2	skiq_tx_hdl_A2
REF	External 40 MHz REF Clock Input	

Table 10: *Sidekiq M.2 NUC RF Ports*

SIDEKIQ M.2 NUC GPIO CONNECTOR

The GPIO connector provides access to monitoring the power supply voltage and current to the mPCIe socket as well as providing access to lines used for digital I/O on the Sidekiq mPCIe. The ability to use a pin as GPIO depends on the loaded FPGA. The connector is a 2x8 header, 0.1" pin spacing, 0.025" square pins (standard size & spacing), Harwin P/N M20-9740846.

Function	Pin	Pin	Function
V_SENSE	1	2	GND
I_SENSE	3	4	GND
M.2 W_DISABLE pin 8	5	6	N/C
N/C	7	8	N/C
GPIO 0 pin 40	9	10	GPIO 1 pin 42
GPIO 2 pin 44	11	12	GPIO 3 pin 46
PPS input only	13	14	GPIO 4 pin 48
N/C	15	16	GND

Table 11: *Sidekiq M.2 NUC 8 GPIO Connector*

V_SENSE: the voltage at the Sidekiq card. Nominally 3.3V.

I_SENSE: outputs a voltage proportional to current in volts/amp, i.e., 0.4 V means the Sidekiq card is drawing 400mA.

Function	Pin	Pin	Function
V_SENSE	1	2	GND
I_SENSE	3	4	GND
W_DISABLE M.2 pin 8	5	6	GND
GPIO_7 M.2 pin 24	7	8	GND
GPIO_0 M.2 pin 40	9	10	GPIO_1 M.2 pin 42
GPIO_2 M.2 pin 44	11	12	GPIO_3 M.2 pin 46
GPIO_5 M.2 pin 20	13	14	GPIO_4 M.2 pin 48
GPIO_6 M.2 pin 22	15	16	GND

Table 12: *Sidekiq M.2 NUC 11 GPIO Connector*

V_SENSE: the voltage at the Sidekiq card. Nominally 3.3V

I_SENSE: outputs a voltage proportional to current in volts/amp, i.e., 0.4 V means the Sidekiq card is drawing 400mA

SIDEKIQ M.2 NUC JTAG CONNECTOR

The JTAG connector is a Samtec P/N STMM-107-02-G-D-RA. It will allow the standard Xilinx 14-pin JTAG cable to be attached.

Function	Pin	Pin	Function
N/C	1	2	VREF*
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	N/C
GND	13	14	N/C

VREF* is a 2.5V output and establishes the required I/O voltage level for the JTAG adapter.

Table 13: *Sidekiq M.2 NUC JTAG Connector*

ACCESSING SIDEKIQ M.2 NUC JTAG CONNECTOR

For customers adding their own custom FPGA blocks in the “user_app” area of the mPCIe Sidekiq reference design, it can often be useful to access JTAG to monitor signals in the FPGA through Xilinx's Chipscope software. The Sidekiq M.2 NUC PDK provides access to the Sidekiq’s JTAG port of the Xilinx Spartan-6 LX45T FPGA through a 2x7 header shown above. A standard Xilinx JTAG USB platform cable, such as the HW-USB-II-G, can be utilized to access JTAG on the FPGA.

APPENDIX A – SIDEKIQ M.2 REV B EDGE CONNECTOR PINOUT

The table below defines the M.2 edge connector pinout for use with the previous revision (Rev B) of Sidekiq M.2. The current Rev C pinout can be found in the M.2 Edge Connector section.

Pin #	M.2 Pin Name	Description as used inSidekiq M.2		Pin #	M.2 Pin Name	Description as used inSidekiq M.2
1	CONFIG_3_	Unused (floating)		39	GND	Ground
2	+3.3V	+3.3V supply		40	GPIO0*	GPIO (FPGA pin G3), 1.8V
3	GND	Ground		41	PERN0	PCIe lane 0 negative leg of receiver diff pair, from host
4	+3.3V	+3.3V supply		42	GPIO1*	GPIO (FPGA pin J3), 1.8V
5	GND	Ground		43	PERP0	PCIe lane 0 positive leg of receiver diff pair, from host
6	FCPO#	Power down control		44	GPIO2*	GPIO (FPGA pin T17), 1.8V
7	USB_D+	USB D+ line		45	GND	Ground
8	W_DISABLE1#	FPGA GPIO #1 to HSC connector (FPGA pin J2), 1.8V		46	GPIO3*	GPIO (FPGA pin H2), 1.8V
9	USB_D-	USB D- line		47	PETN0	PCIe lane 0 negative leg of transmitter diff pair, to host
10	GPIO9	Unused (floating)		48	GPIO4	GPIO (FPGA pin T18), 1.8V
11	GND	Ground		49	PETP0	PCIe lane 0 positive leg of transmitter diff pair, to host
12	Key	N/A (Module B key)		50	PERST#	Unused
13	Key	N/A (Module B key)		51	GND	Ground
14	Key	N/A (Module B key)		52	CLKREQ#	Clock Request, pulled low whenever Sidekiq M.2 is powered up
15	Key	N/A (Module B key)		53	REFCLKN	PCIe reference clock negative leg of diff pair, from host
16	Key	N/A (Module B key)		54	PEWAKE#	Unused (floating)
17	Key	N/A (Module B key)		55	REFCLKP	PCIe reference clock positive leg of diff pair, from host
18	Key	N/A (Module B key)		56	N/C	Pull low to enable JTAG I/O buffers
19	Key	N/A (Module B key)		57	GND	Ground
20	GPIO5	GPIO (FPGA pin J18), 1.8V		58	N/C	Pull high to enable JTAG I/O buffers
21	CONFIG_0	Unused (floating)		59	ANTCTL0	GPIO (FPGA pin C15), 1.8V

22	GPIO6	Unused (floating)		60	COEX3	GPIO (FPGA pin P19), 1.8V
23	GPIO11	Unused (floating)		61	ANTCTL1	Unused (floating)
24	GPIO7	Unused (floating)		62	COEX2	RFIC_SYNC (1.8V input), used to synchronize multiple cards
25	DPR	Unused (floating)		63	ANTCTL2	Unused (floating)
26	GPIO10	Unused (floating)		64	COEX1**	PPS input to FPGA (1.8V input)
27	GND	Ground		65	ANTCTL3	Unused (floating)
28	GPIO8	Unused (floating)		66	SIM_DET	Unused (floating)
29	PERN1	Unused (floating)		67	RESET#	1.8V I/O, hard reset when low
30	UIM-RESET	JTAG TMS line for FPGA		68	SUSCLK	Unused (floating)
31	PERP1	Unused (floating)		69	CONFIG_1	Unused (floating)
32	UIM-CLK	JTAG TDO line for FPGA		70	3.3V	3.3V from host to power card
33	GND	Ground		71	GND	Ground
34	UIM-DATA	JTAG TDI line for FPGA		72	3.3V	3.3V from host to power card
35	PETN1	Unused (floating)		73	GND	Ground
36	UIM-PWR	JTAG TCK line for FPGA		74	3.3V	3.3V from host to power card
37	PETP1	Unused (floating)		75	CONFIG_2	Pulled low through resistor to ground
38	DEVSLP	Unused (floating)		76	N/C	Unused (floating)

Table 14: *M.2 edge connector pinout for Rev B cards*

APPENDIX B – SIDEKIQ M.2 STATEMENT OF VOLATILITY

Model	Sidekiq M.2
Part Number	ES014-103
Manufacturer	Epiq Solutions
Address	3740 Industrial Avenue Rolling Meadows, IL 60008

Table 15: *Model, Part Number, and Manufacturer Info*

Memory Type	Memory Size	User Modifiable	Purpose	Process to Clear
On-Chip FPGA BRAM	13 Mbit	Yes	Application usage	Power-off

Table 16: *Sidekiq M.2 Volatile Memory*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
Flash	64 Mbit	Yes	No	Holds the FPGA bitstream	Cleared via API
EEPROM	16 KB	Yes	No	Contains product information for identifying the device (part#, serial#). User configuration settings (ref_clock). USB controller firmware	Product information and USB controller firmware are read only and must be returned to factory to be cleared. ref_clock setting is read/write via the API.

Table 17: *Sidekiq M.2 Non-Volatile Memory*

APPENDIX C – FAILURE RATE & MTBF

Listed below are the failure rates and MTBFs for the ES014-203-C Sidekiq M.2 001 and ES014-200-C Sidekiq M.2 002 assemblies.

The calculations are derived from Relyence Reliability Software and based off a fixed/ground/controlled operating environment with an ambient temperature of 25°C.

Part Number	ES014-203-C
Description	Sidekiq M.2 001
Failure Rate (fpmh)	1.325499
MTBF (hours)	754432.88
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 18: *Sidekiq M.2 001 Failure Rate & MTBF*

Part Number	ES014-200-C
Description	Sidekiq M.2 002
Failure Rate (fpmh)	1.237856
MTBF (hours)	807848.30
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 19: *Sidekiq M.2 002 Failure Rate & MTBF*